# 3-17V 3A Step-Down Converter in 3x3 QFN Package

**Check for Samples: TPS62130, TPS62131, TPS62132, TPS62133**

## FEATURES

- **DCS-Control™ Topology**
- **Input Voltage Range: 3 to 17V**
- **Up to 3A Output Current**
- **Adjustable Output Voltage from 0.9 to 6V**
- **Pin-Selectable Output Voltage (nominal, + 5%)**
- **Programmable Soft Start and Tracking**
- **Seamless Power Save Mode Transition**
- **Quiescent Current of 17µA (typ.)**
- **Selectable Operating Frequency**
- **Power Good Output**
- **100% Duty Cycle Mode**
- **Short Circuit Protection**
- **Over Temperature Protection**
- **Available in a 3 × 3 mm, QFN-16 Package**

## APPLICATIONS

- **Standard 12V Rail Supplies**
- **POL Supply from Single or Multiple Li-Ion Battery**
- **Solid-State Disk Drives**
- **Embedded Systems**
- **LDO replacement**
- **Mobile PC's, Tablet, Modems, Cameras**

## DESCRIPTION

The TPS6213X family is an easy to use synchronous step down DC-DC converter optimized for applications with high power density. A high switching frequency of typically 2.5MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilization of the DCS-Control™ topology.

With its wide operating input voltage range of 3V to 17V, the devices are ideally suited for systems powered from either a Li-Ion or other batteries as well as from 12V intermediate power rails. It supports up to 3A continuous output current at output voltages between 0.9V and 6V (with 100% duty cycle mode).

The output voltage startup ramp is controlled by the soft-start pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the Enable and open-drain Power Good pins.

In Power Save Mode, the devices show quiescent current of about 17µA from VIN. Power Save Mode, entered automatically and seamlessly if load is small, maintains high efficiency over the entire load range. In Shutdown Mode, the device is turned off and shutdown current consumption is less than 2µA.

The device, available in adjustable and fixed output voltage versions, is packaged in a 16-pin QFN package measuring 3 × 3 mm (RGT).

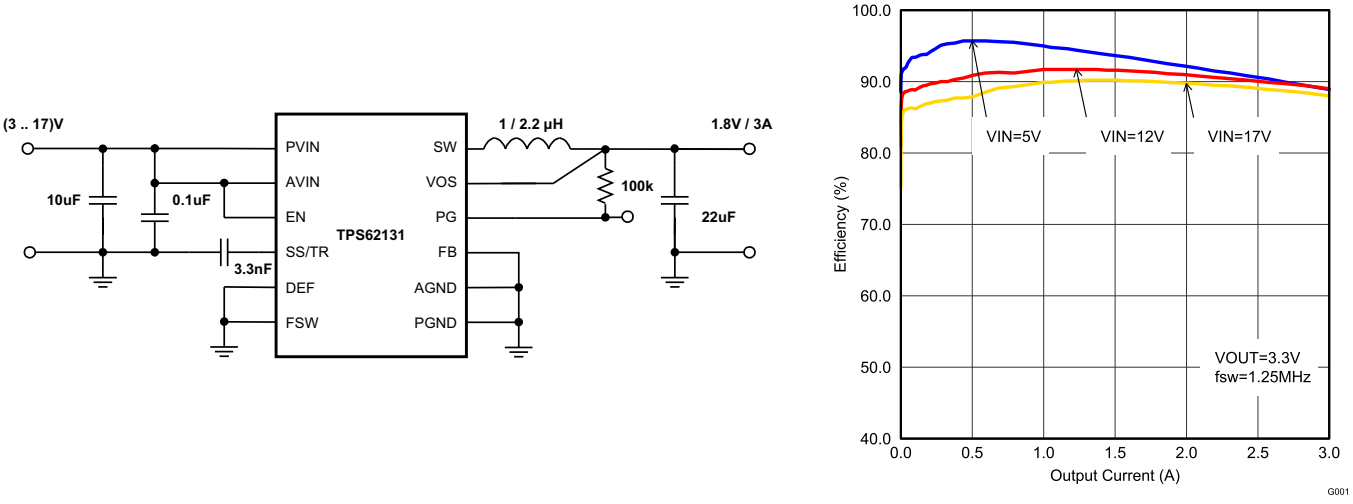



**Figure 1. Typical Application and Efficiency**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| $T_A$ | OUTPUT VOLTAGE | PART NUMBER(2) | PACKAGE | ORDERING | PACKAGE MARKING |
|---|---|---|---|---|---|
| -40°C to 85°C | adjustable | TPS62130 | 16-Pin QFN | TPS62130RGT | PTSI |
| | 1.8 V | TPS62131 | | TPS62131RGT | QVX |
| | 3.3 V | TPS62132 | | TPS62132RGT | QVY |
| | 5.0 V | TPS62133 | | TPS62133RGT | QVZ |

(1) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.
(2) Contact the factory to check availability of other fixed output voltage versions.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Pin voltage range(2) | AVIN, PVIN | –0.3 | 20 | V |
| | EN, SS/TR | –0.3 | $V_{IN}$+0.3 | |
| | SW | –0.3 | $V_{IN}$+0.3 | V |
| | DEF, FSW, FB, PG, VOS | –0.3 | 7 | V |
| Power Good sink current | PG | | 10 | mA |
| Temperature range | Operating junction temperature range, $T_J$ | –40 | 125 | °C |
| | Storage temperature range, $T_{stg}$ | –65 | 150 | |
| ESD rating(3) | HBM Human body model | | 2 | kV |
| | CDM Charge device model | | 0.5 | kV |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS6213X RGT 16 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 29.1 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case(top) thermal resistance | 15 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 11 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 10 | |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case(bottom) thermal resistance | 3.5 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage, $V_{IN}$ (at AVIN and PVIN) | 3 | | 17 | V |
| Operating free air temperature, $T_A$ | –40 | | 85 | °C |
| Operating junction temperature, $T_J$ | –40 | | 125 | °C |


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## ELECTRICAL CHARACTERISTICS

over free-air temperature range ($T_A$=-40°C to +85°C), typical values at $V_{IN}$=12V and $T_A$=25°C (unless otherwise noted)

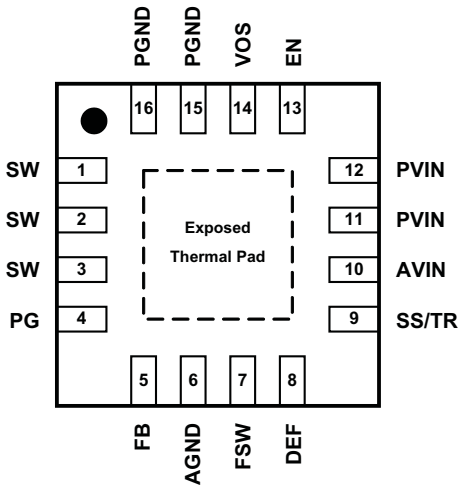
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $V_{IN}$ | Input voltage range(1) | | 3 | | 17 | V |
| $I_Q$ | Operating quiescent current | EN=High, $I_{OUT}$=0mA, device not switching | | 17 | 25 | µA |
| $I_{SD}$ | Shutdown current(2) | EN=Low | | 1.5 | 4 | µA |
| $V_{UVLO}$ | Undervoltage lockout threshold | Falling Input Voltage | 2.6 | 2.7 | 2.8 | V |
| | | Hysteresis | | 200 | | mV |
| $T_{SD}$ | Thermal shutdown temperature | | | 160 | | °C |
| | Thermal shutdown hysteresis | | | 20 | | |
| **CONTROL (EN, DEF, FSW, SS/TR, PG)** | | | | | | |
| $V_H$ | High level input threshold voltage (EN, DEF, FSW) | | 0.9 | | | V |
| $V_L$ | Low level input threshold voltage (EN, DEF, FSW) | | | | 0.3 | V |
| $I_{LKG}$ | Input leakage current (EN, DEF, FSW) | EN=$V_{IN}$ or GND; DEF, FSW=$V_{OUT}$ or GND | | 0.01 | 1 | µA |
| $V_{TH_PG}$ | Power good threshold voltage | Rising (%$V_{OUT}$) | 92 | 95 | 98 | % |
| | | Falling (%$V_{OUT}$) | 87 | 90 | 94 | |
| $V_{OL_PG}$ | Power good output low | $I_{PG}$=-2mA | | 0.07 | 0.3 | V |
| $I_{LKG_PG}$ | Input leakage current (PG) | $V_{PG}$=1.8V | | 1 | 400 | nA |
| $I_{SS/TR}$ | SS/TR pin source current | | 2.3 | 2.5 | 2.7 | µA |
| **POWER SWITCH** | | | | | | |
| $R_{DS(ON)}$ | High-side MOSFET ON-resistance | $V_{IN}$≥6V | | 90 | 170 | mΩ |
| | | $V_{IN}$=3V | | 120 | | |
| | Low-side MOSFET ON-resistance | $V_{IN}$≥6V | | 40 | 70 | mΩ |
| | | $V_{IN}$=3V | | 50 | | |
| $I_{LIMF}$ | High-side MOSFET forward current limit(3) | $V_{IN}$ =12V, $T_A$= 25°C | 3.6 | 4.2 | 4.9 | A |
| **OUTPUT** | | | | | | |
| VREF | Internal reference voltage(4) | | | 0.8 | | V |
| $I_{LKG_FB}$ | Input leakage current (FB) | TPS62130, $V_{FB}$=0.8V | | 1 | 100 | nA |
| $V_{OUT}$ | Output voltage range (TPS62130) | $V_{IN}$ ≥ $V_{OUT}$ | 0.9 | | 6.0 | V |
| | DEF (Output voltage programming) | DEF=0 (GND) | | VOUT | | |
| | | DEF=1 ($V_{OUT}$) | | VOUT+5% | | |
| | Initial output voltage accuracy(5) | PWM mode operation, $V_{IN}$ ≥ $V_{OUT}$ +1V | –1.8 | | 1.8 | % |
| | | Power Save Mode operation, $C_{OUT}$=22µF | -2.3 | | 2.8 | |
| | Load regulation(6) | $V_{IN}$=12V, $V_{OUT}$=3.3V, PWM mode operation | | 0.05 | | %/A |
| | Line regulation(6) | 3V ≤ $V_{IN}$ ≤ 17V, $V_{OUT}$=3.3V, $I_{OUT}$= 1A, PWM mode operation | | 0.02 | | %/V |

(1) The device is still functional down to Under Voltage Lockout (see parameter $V_{UVLO}$).
(2) Current into AVIN+PVIN pin.
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see Current Limit And Short Circuit Protection section).
(4) This is the voltage regulated at the FB pin.
(5) This is the accuracy provided by the device itself (line and load regulation effects are not included). For the fixed voltage versions the (internal) resistive divider is included.
(6) Line and load regulation depend on external component selection and layout (see Figure 17 and Figure 18).

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## DEVICE INFORMATION

**RGT PACKAGE**
**(TOP VIEW)**




### Terminal Functions

| PIN(1) | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SW | 1,2,3 | O | Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor. |
| PG | 4 | O | Output power good (High = VOUT ready, Low = VOUT below nominal regulation) ; open drain (requires pull-up resistor; goes high impedance, when device is switched off) |
| FB | 5 | I | Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance. |
| AGND | 6 | | Analog Ground |
| FSW | 7 | I | Switching Frequency Select (Low ≈ 2.5MHz, High ≈ 1.25MHz for typical operation)(2) |
| DEF | 8 | I | Output Voltage Scaling (Low = nominal, High = nominal + 5%)(2) |
| SS/TR | 9 | I | Soft-Start / Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing. |
| AVIN | 10 | I | Supply voltage for control circuitry. Connect to same source as PVIN. |
| PVIN | 11,12 | I | Supply voltage for power stage. Connect to same source as AVIN. |
| EN | 13 | I | Enable input (High = enabled, Low = disabled)(2) |
| VOS | 14 | I | Output voltage sense pin and connection for the control loop circuitry. |
| PGND | 15,16 | | Power ground |
| Exposed Thermal Pad | | | Must be connected to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability. |

(1) For more information about connecting pins, see DETAILED DESCRIPTION and APPLICATION INFORMATION sections.
(2) An internal pull-down resistor keeps logic level low, if pin is floating.


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## FUNCTIONAL BLOCK DIAGRAM

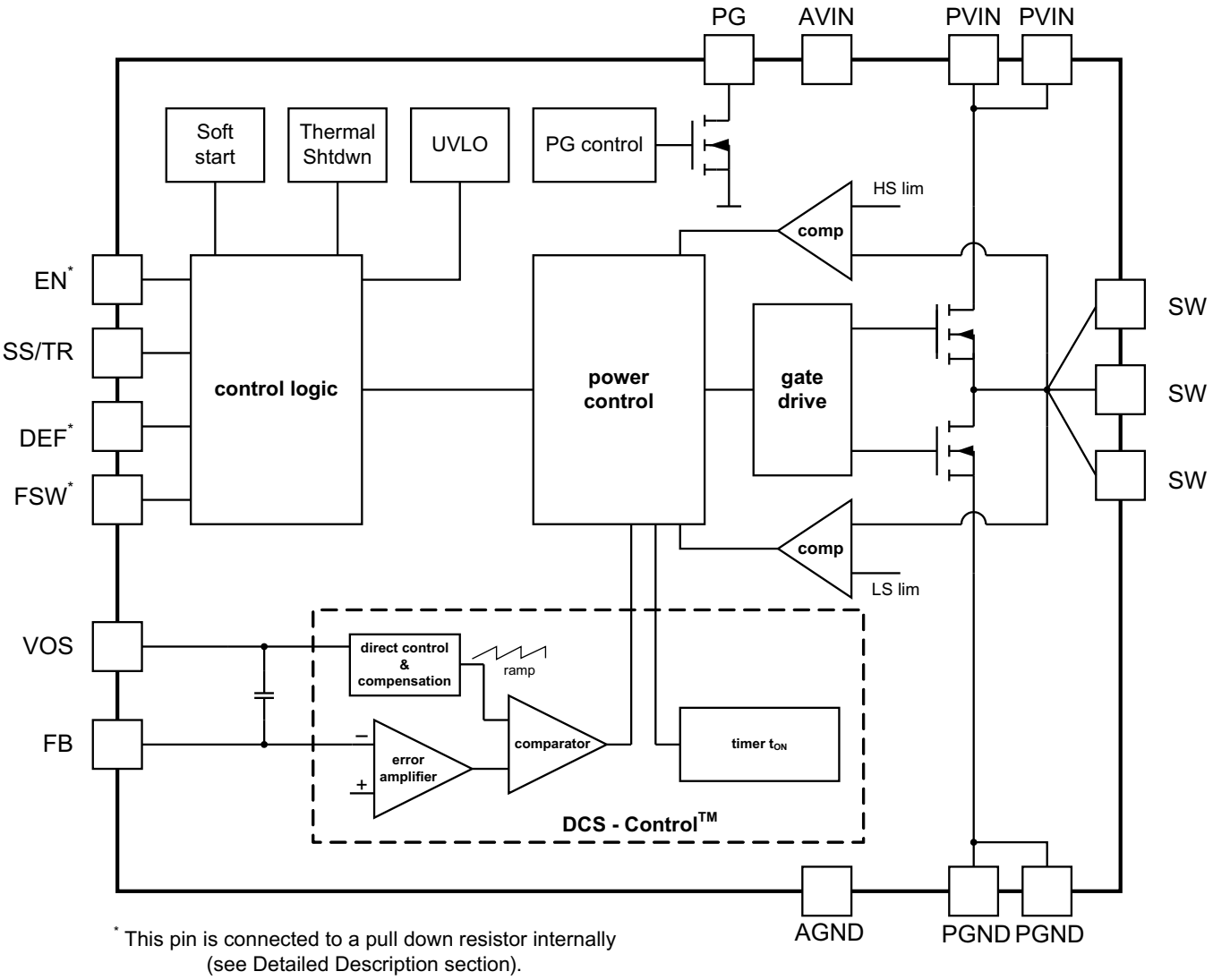



**Figure 2. TPS62130 (adjustable output voltage)**

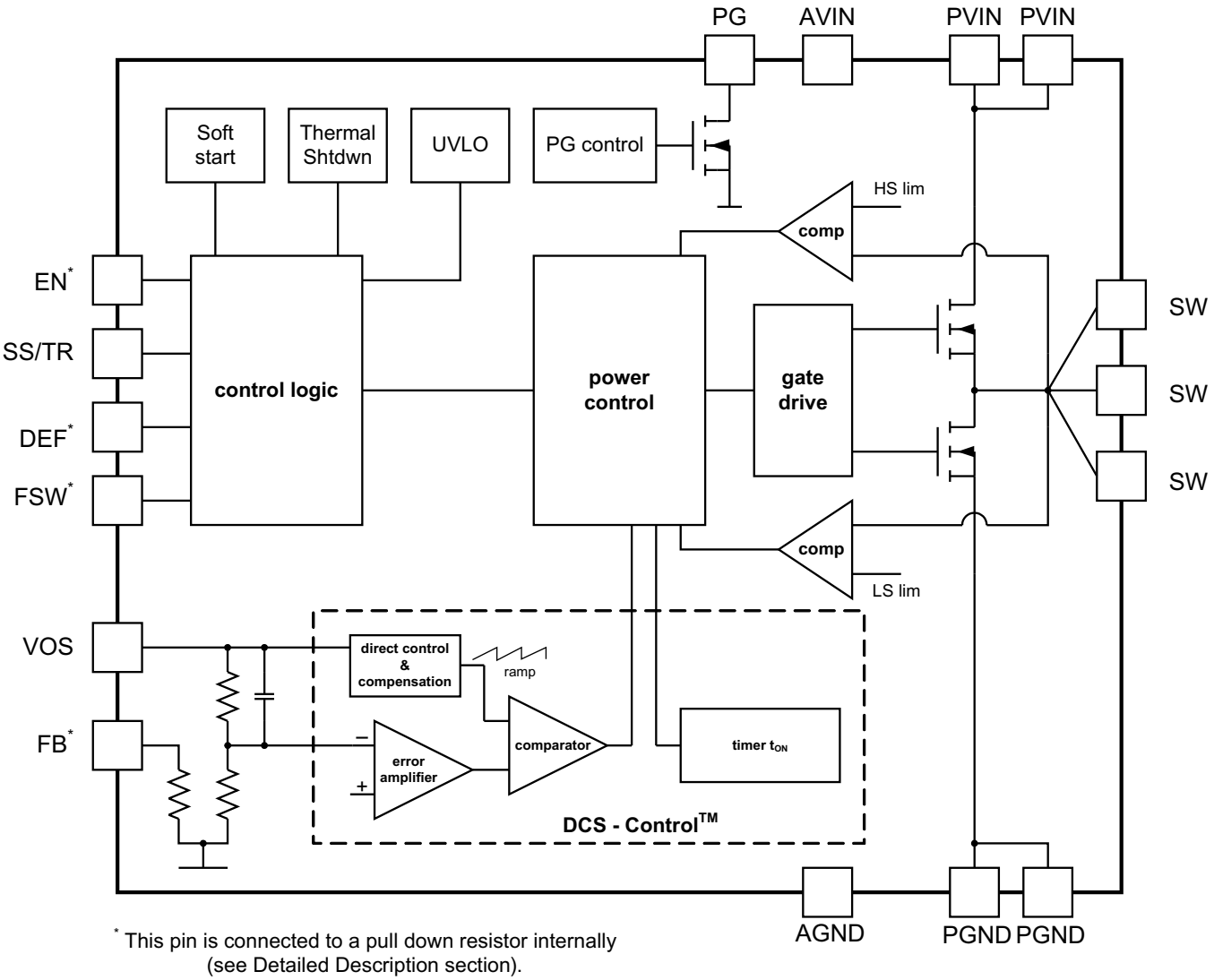



**Figure 3. TPS62131/2/3 (fixed output voltage)**


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## PARAMETER MEASUREMENT INFORMATION

### List of Components

| REFERENCE | DESCRIPTION | MANUFACTURER |
|---|---|---|
| IC | 17V, 3A Step-Down Converter, QFN | TPS62130RGT, Texas Instruments |
| L1 | 2.2µH, 0.165 x 0.165 in | XFL4020-222MEB, Coilcraft |
| Cin | 10µF, 25V, Ceramic | Standard |
| Cout | 22µF, 6.3V, Ceramic | Standard |
| Cs | 3300pF, 25V, Ceramic | |
| R1 | depending on Vout | |
| R2 | depending on Vout | |
| R3 | 100kΩ, Chip, 0603, 1/16W, 1% | Standard |

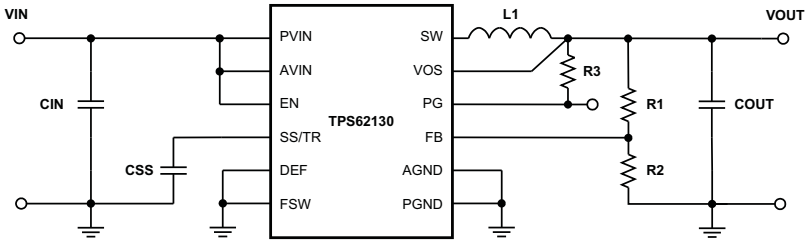



**Figure 4. Measurement Setup**

## TYPICAL CHARACTERISTICS

### Table of Graphs

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|---|---|---|
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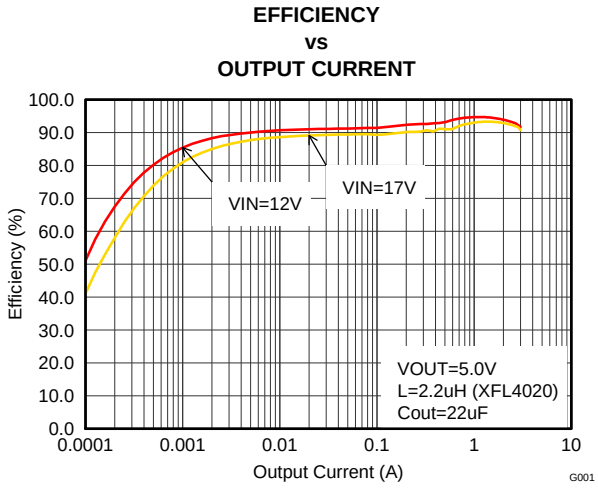



Figure 5. Efficiency with 1.25MHz, Vout=5V

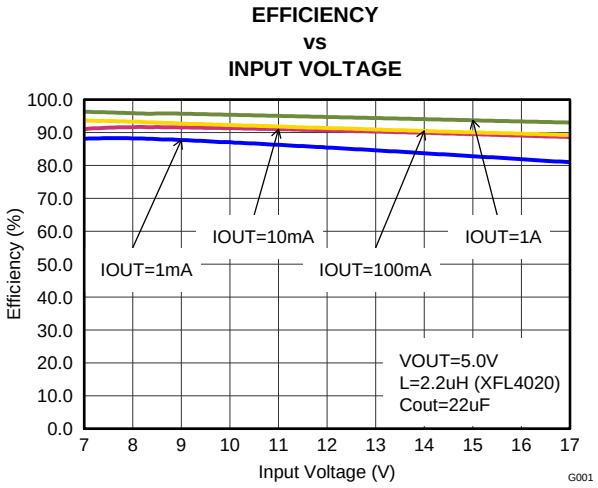



Figure 6. Efficiency with 1.25MHz, Vout=5V

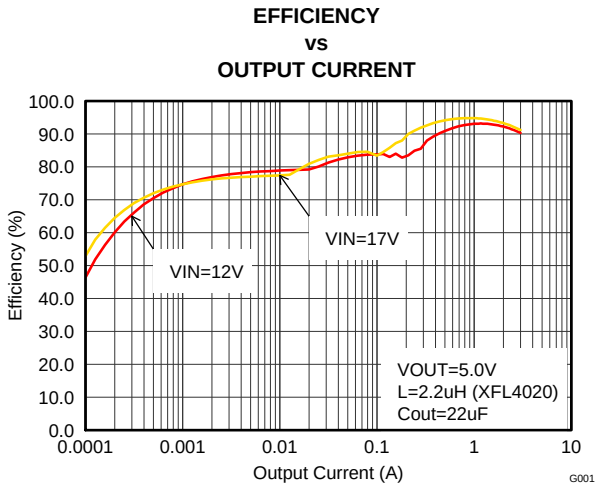



Figure 7. Efficiency with 2.5MHz, Vout=5V

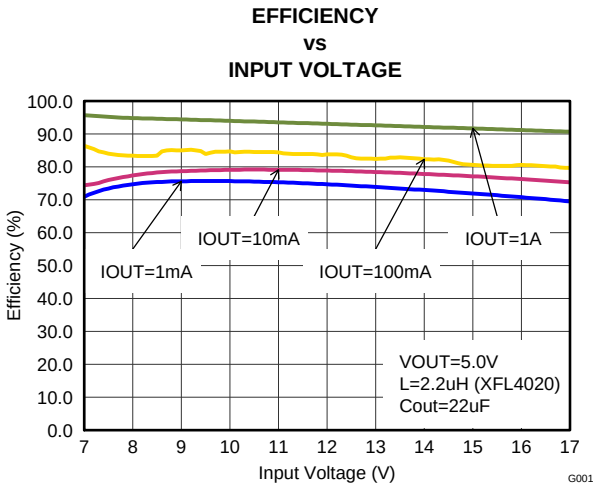



Figure 8. Efficiency with 2.5MHz, Vout=5V

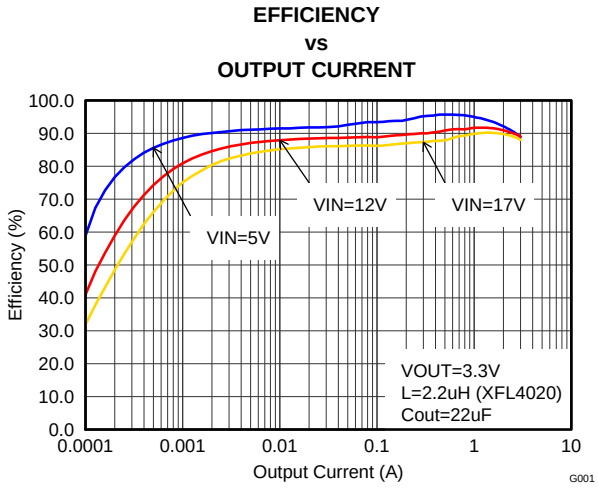



Figure 9. Efficiency with 1.25MHz, Vout=3.3V

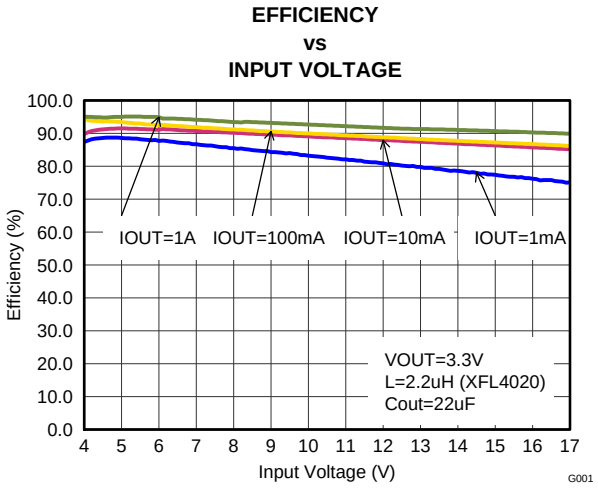



Figure 10. Efficiency with 1.25MHz, Vout=3.3V


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**EFFICIENCY vs OUTPUT CURRENT**

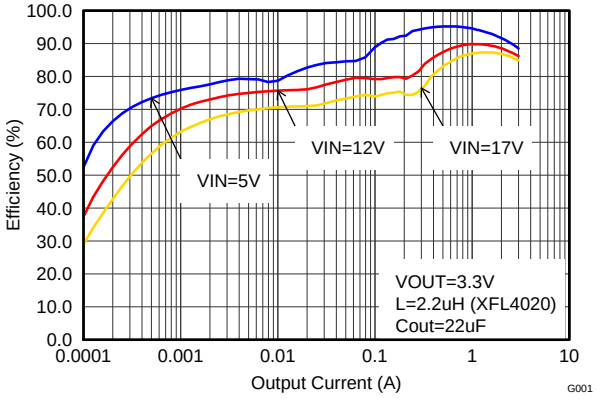



**Figure 11. Efficiency with 2.5MHz, Vout=3.3V**

**EFFICIENCY vs INPUT VOLTAGE**

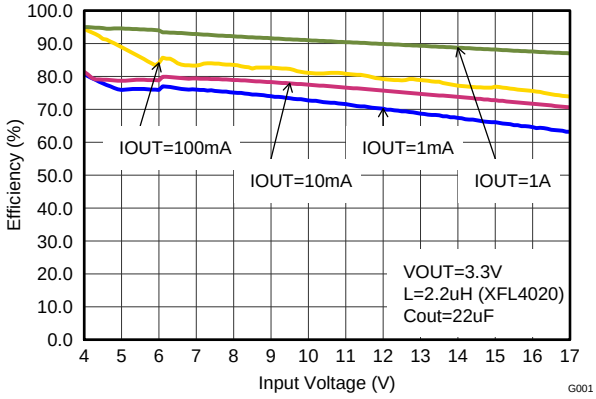



**Figure 12. Efficiency with 2.5MHz, Vout=3.3V**

**EFFICIENCY vs OUTPUT CURRENT**

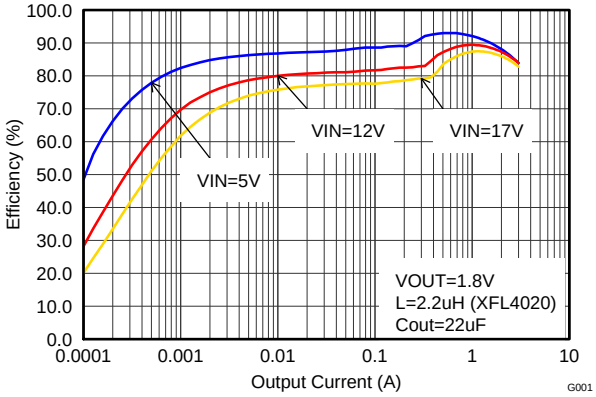



**Figure 13. Efficiency with 1.25MHz, Vout=1.8V**

**EFFICIENCY vs INPUT VOLTAGE**

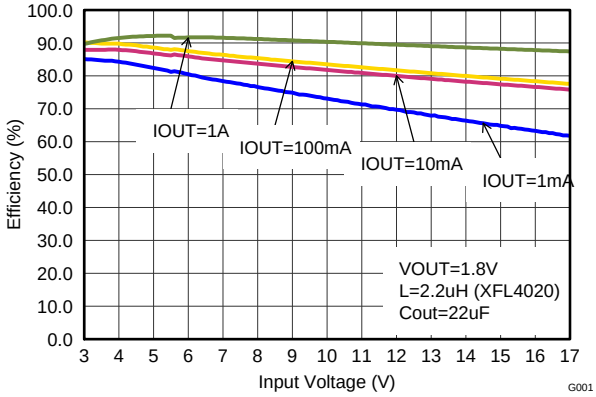



**Figure 14. Efficiency with 1.25MHz, Vout=1.8V**

**EFFICIENCY vs OUTPUT CURRENT**

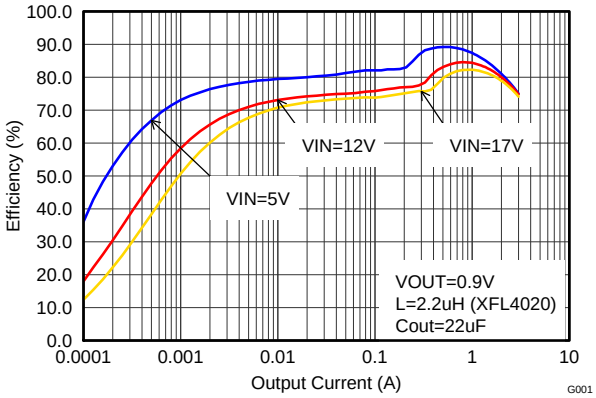



**Figure 15. Efficiency with 1.25MHz, Vout=0.9V**

**EFFICIENCY vs INPUT VOLTAGE**

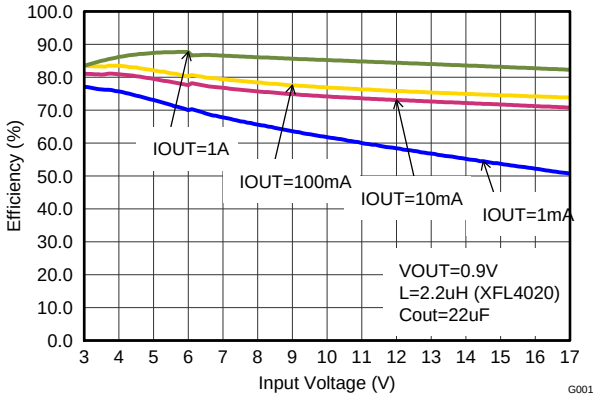



**Figure 16. Efficiency with 1.25MHz, Vout=0.9V**

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**OUTPUT VOLTAGE vs OUTPUT CURRENT**

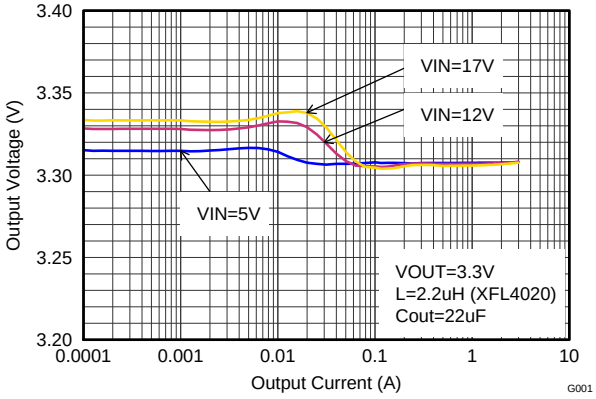



**Figure 17. Output Voltage Accuracy (Load Regulation)**

**OUTPUT VOLTAGE vs INPUT VOLTAGE**

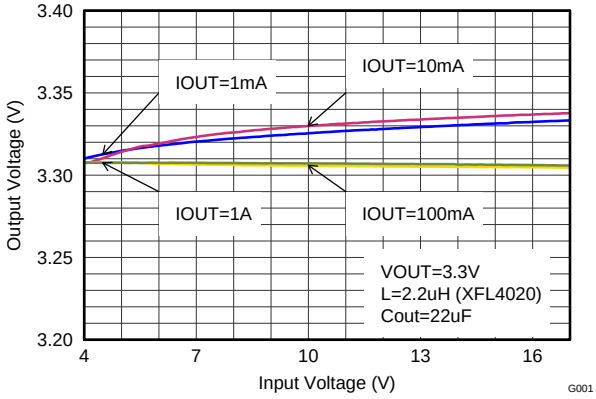



**Figure 18. Output Voltage Accuracy (Line Regulation)**

**SWITCHING FREQUENCY vs INPUT VOLTAGE**

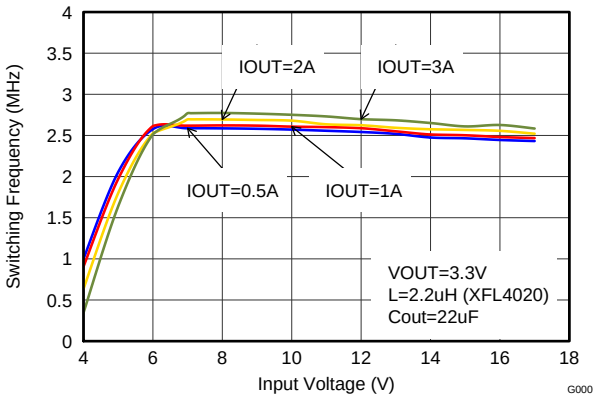



**Figure 19. Switching Frequency**

**SWITCHING FREQUENCY vs OUTPUT CURRENT**

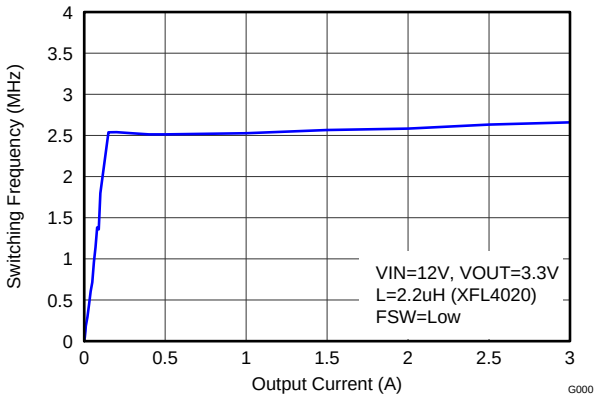



**Figure 20. Switching Frequency**

**INPUT CURRENT vs INPUT VOLTAGE**

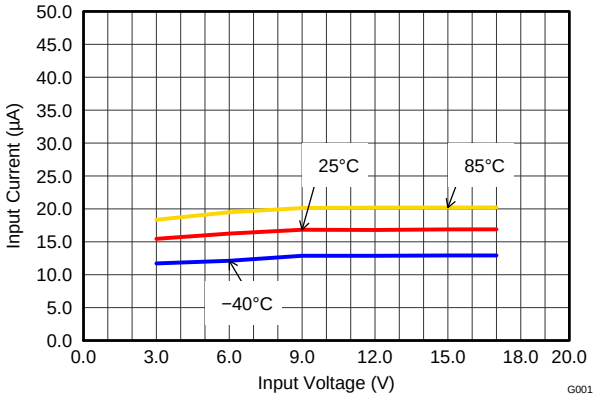



**Figure 21. Quiescent Current**

**INPUT CURRENT vs INPUT VOLTAGE**

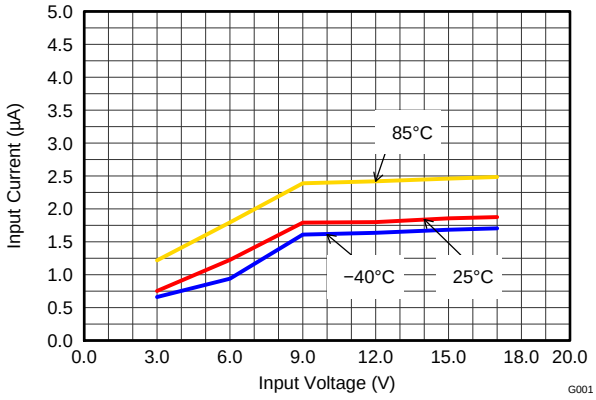



**Figure 22. Shutdown Current**


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**STATIC DRAIN-SOURCE-RESISTANCE ($R_{DSon}$) vs INPUT VOLTAGE**

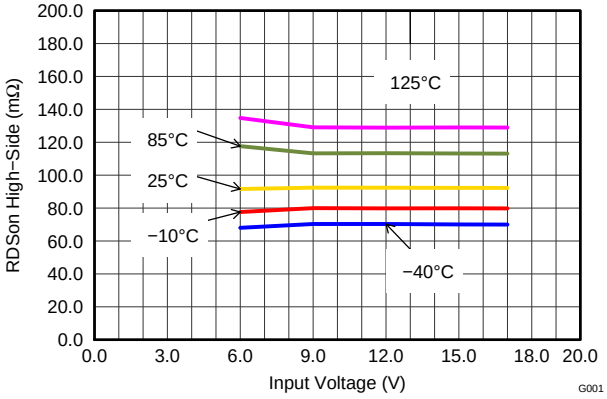



**Figure 23. High-Side Switch Resistance**

**STATIC DRAIN-SOURCE-RESISTANCE ($R_{DSon}$) vs INPUT VOLTAGE**

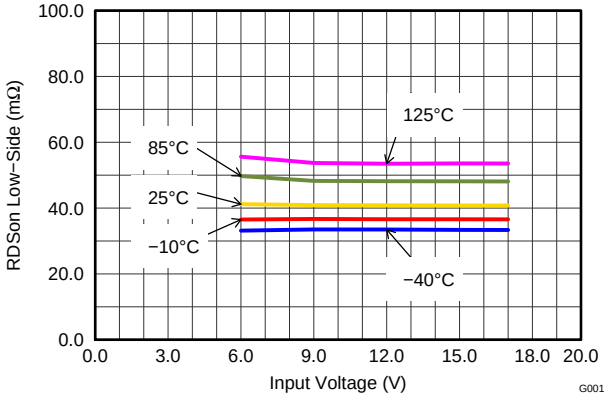



**Figure 24. Low-Side Switch Resistance**

**OUTPUT VOLTAGE vs OUTPUT CURRENT**

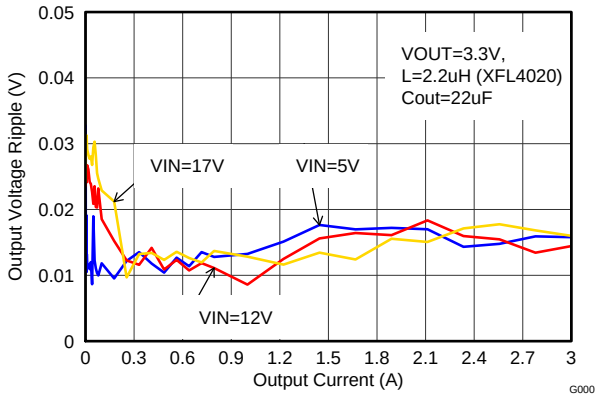



**Figure 25. Output Voltage Ripple**

**OUTPUT CURRENT vs INPUT VOLTAGE**

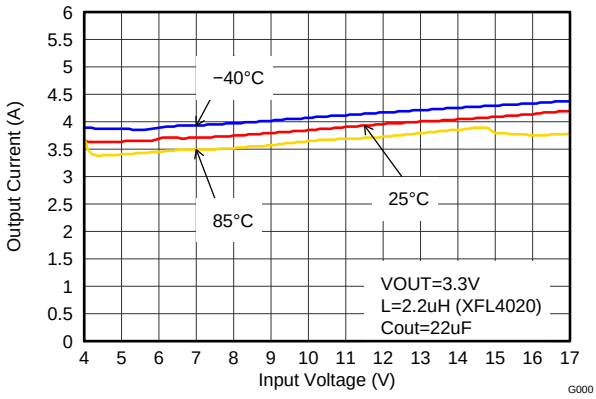



**Figure 26. Maximum Output Current**

**POWER SUPPLY REJECTION RATIO vs FREQUENCY**

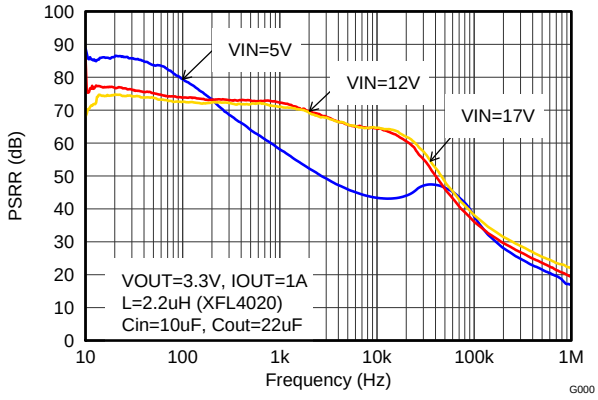



**Figure 27. Power Supply Rejection Ratio, $f_{SW}$=2.5MHz**

**POWER SUPPLY REJECTION RATIO vs FREQUENCY**

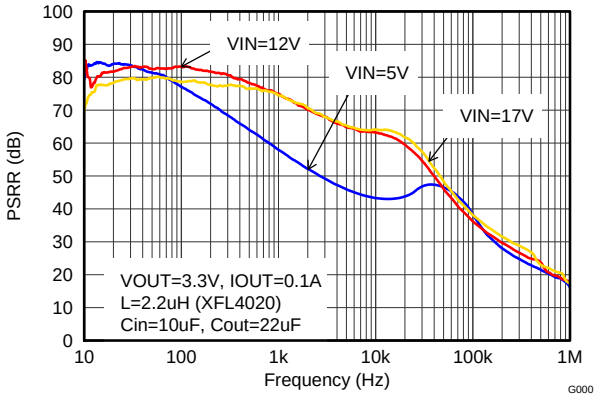



**Figure 28. Power Supply Rejection Ratio, $f_{SW}$=2.5MHz**

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OUTPUT VOLTAGE
vs
TIME

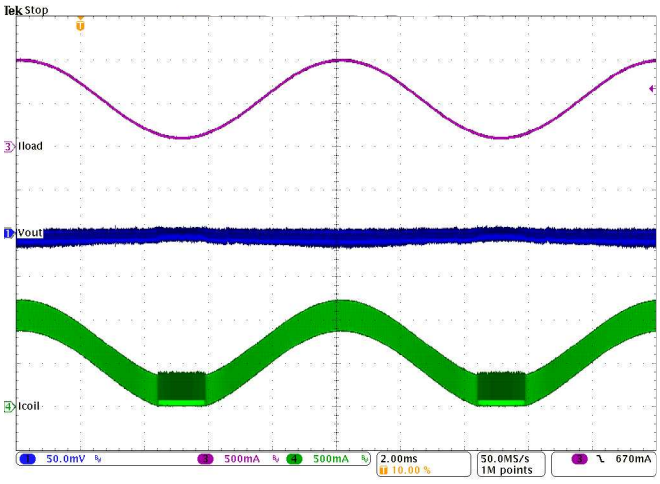



Figure 29. PWM-PSM-Transition ($V_{IN}$=12V, $V_{OUT}$=3.3V with 50mV/div)

OUTPUT VOLTAGE
vs
TIME

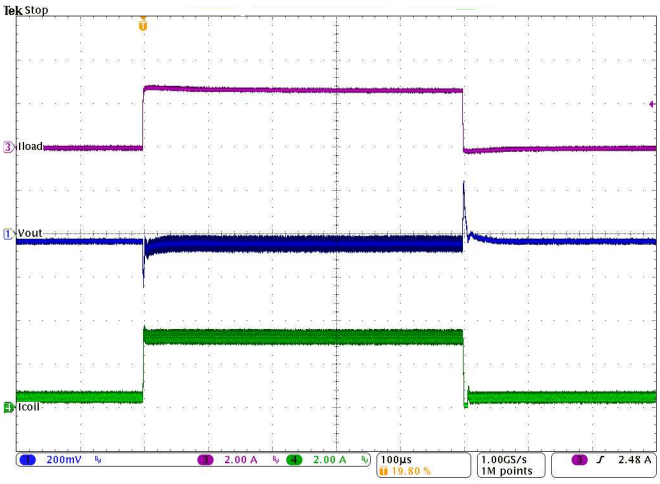



Figure 30. Load Transient Response ($I_{OUT}$= 0.5 to 3 to 0.5 A, $V_{IN}$=12V, $V_{OUT}$=3.3V)

OUTPUT VOLTAGE
vs
TIME

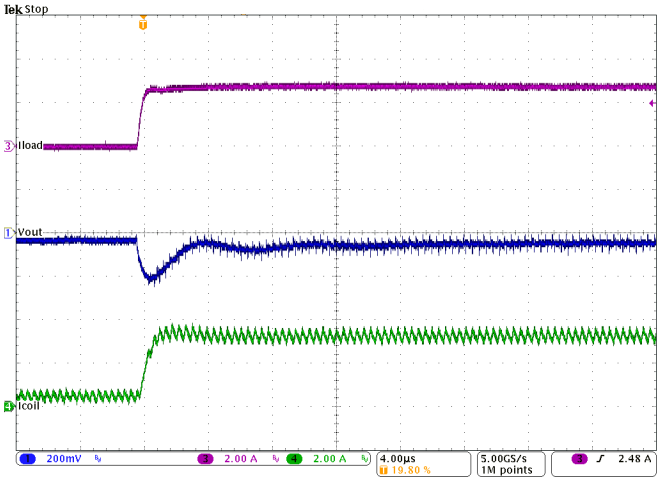



Figure 31. Load Transient Response of Figure 30, rising edge

OUTPUT VOLTAGE
vs
TIME

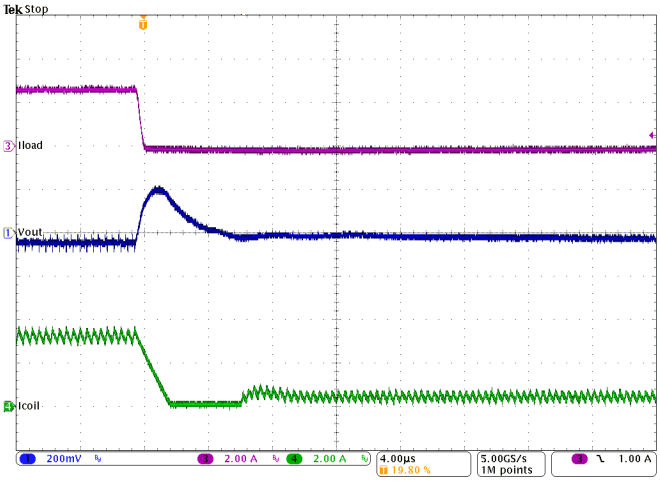



Figure 32. Load Transient Response of Figure 30, falling edge


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**OUTPUT VOLTAGE vs TIME**

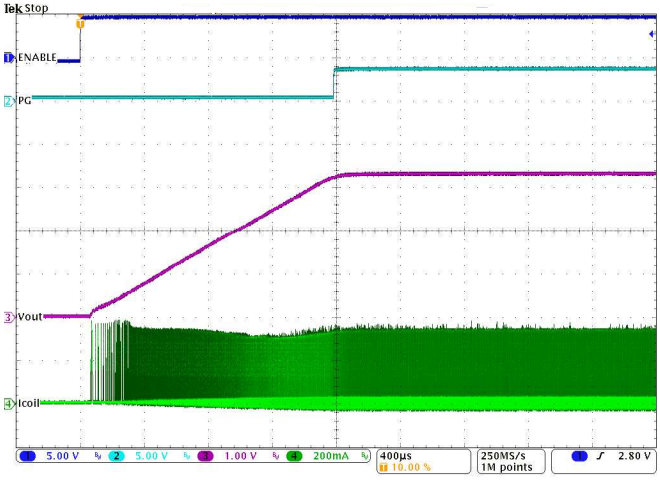



**Figure 33. Startup into 100mA (VIN=12V, VOUT=3.3V)**

**OUTPUT VOLTAGE vs TIME**

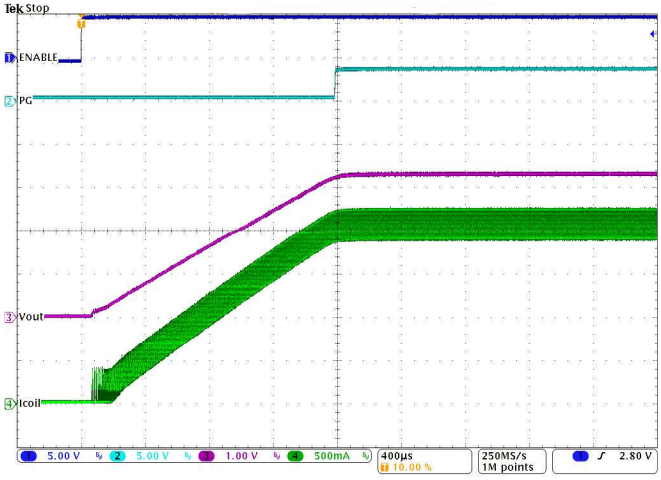



**Figure 34. Startup into 3A (VIN=12V, VOUT=3.3V)**

**PWM SIGNALS vs TIME**

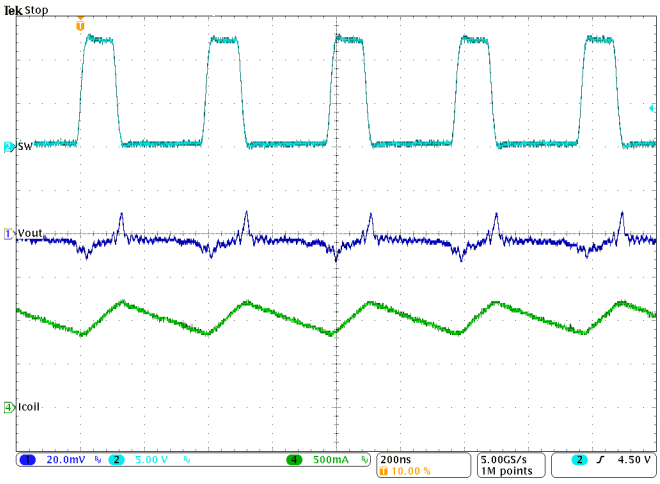



**Figure 35. Typical Operation in PWM Mode ($I_{OUT}$=1A)**

**POWER SAVE MODE SIGNALS vs TIME**

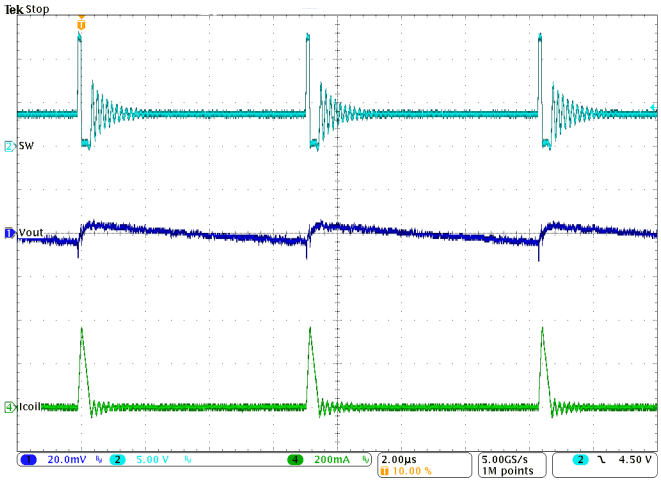



**Figure 36. Typical Operation in Power Save Mode ($I_{OUT}$=10mA)**

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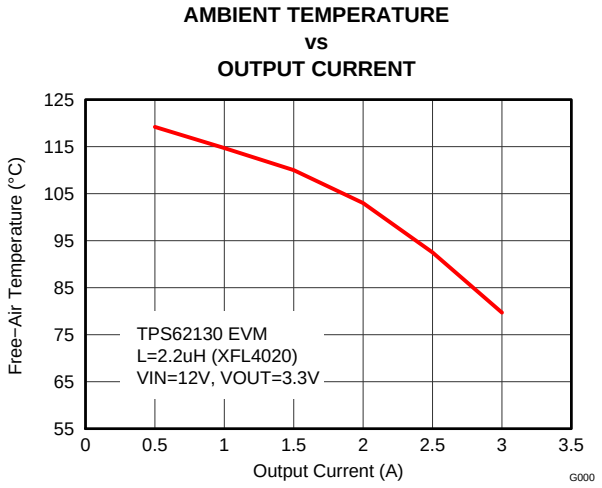



**Figure 37. Maximum Ambient Temperature ($f_{SW}$=2.5MHz)**

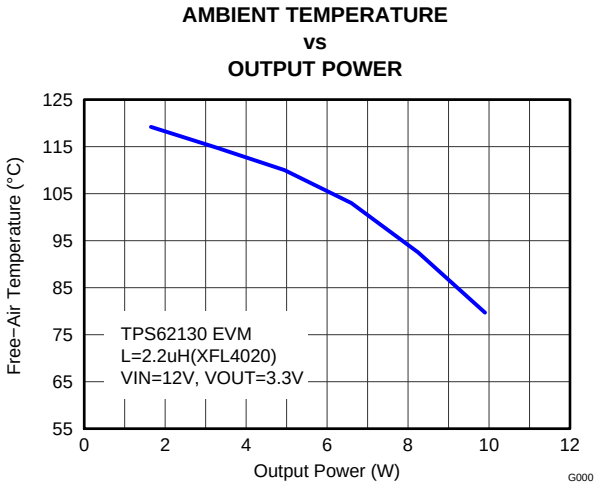



**Figure 38. Maximum Ambient Temperature ($f_{SW}$=2.5MHz)**


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## DETAILED DESCRIPTION

### Device Operation

The TPS6213X synchronous switched mode power converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

Fixed output voltage versions provide smallest solution size and lowest current consumption, requiring only 3 external components. An internal current limit supports nominal output currents of up to 3A.

The TPS6213X family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

### Pulse Width Modulation (PWM) Operation

The TPS6213X operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on $V_{IN}$, $V_{OUT}$ and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

### Power Save Mode Operation

The TPS6213X's built in Power Save Mode will be entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

TPS6213X includes a fixed on-time circuitry. This on-time, in steady-state operation, can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 400ns \tag{1}$$

For very small output voltages, an absolute minimum on-time of about 80ns is kept to limit switching losses. Using $t_{ON}$, the typical peak inductor current in Power Save Mode can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \tag{2}$$

When $V_{IN}$ decreases to typically 15% above VOUT, the TPS6213X won't enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

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### 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D=Vout/Vin and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, e.g. for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \quad (3)$$

where

$I_{OUT}$ is the output current,
$R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET and
$R_L$ is the DC resistance of the inductor used.

### Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation.

Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. An internal pull-down resistor of about 400kΩ is connected and keeps EN logic low, if the pin is floating. It is disconnected if the pin is High.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

### Soft Start / Tracking (SS/TR)

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50µs and VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin. See Figure 33 and Figure 34 for typical startup operation.

Connecting SS/TR directly to AVIN provides fastest startup behavior. The TPS6213X can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage. As long as the output is below about 0.5V a reduced current limit of typically 1.6A is set internally. If the device is set to shutdown (EN=GND), undervoltage lockout or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new startup sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage will follow this voltage in both directions up and down (see APPLICATION INFORMATION).

### Current Limit And Short Circuit Protection

The TPS6213X devices are protected against heavy load and short circuit events. If a short circuit is detected (VOUT drops below 0.5V), the current limit is reduced to 1.6A typically. If the output voltage rises above 0.5V, the device will run in normal operation again. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET will be turned off. Avoiding shoot through current, the low-side FET will be switched on to sink the inductor current. The high-side FET will turn on again, only if the current in the low-side FET has decreased below the low side current limit threshold.

The output current of the device is limited by the current limit (see ELECTRICAL CHARACTERISTICS). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:


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$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD} \quad (4)$$

where

$I_{LIMF}$ is the static current limit, specified in the ELECTRICAL CHARACTERISTICS,
L is the inductor value,
$V_L$ is the voltage across the inductor ($V_{IN}$ - $V_{OUT}$) and
$t_{PD}$ is the internal propagation delay.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \quad (5)$$

## Power Good (PG)

The TPS6213X has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7V). It can sink 2mA of current and maintain its specified logic low level. It is high impedance when the device is turned off due to EN, UVLO or thermal shutdown.

## Pin-Selectable Output Voltage (DEF)

The output voltage of the TPS6213X devices can be increased by 5% above the nominal voltage by setting the DEF pin to High(1). When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using TPS6213X can be found in SLVA489. A pull down resistor of about 400kOhm is internally connected to the pin, to ensure a proper logic level if the pin is high impedance or floating. The resistor is disconnected if the pin is High.

## Frequency Selection (FSW)

To get high power density with very small solution size, a high switching frequency allows the use of small external components for the output filter. However switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typ.) by pulling FSW to High(1). Pull FSW to Low for high frequency operation (2.5 MHz typ.). Running with lower frequency a higher efficiency, but also a higher output voltage ripple, is achieved. To get low ripple and full output current at the lower switching frequency, it's recommended to use an inductor of at least 2.2uH. The switching frequency can be changed during operation, if needed. A pull down resistor of about 400kOhm is internally connected to the pin, to ensure a proper logic level if the pin is high impedance or floating. The resistor is disconnected if the pin is High.

## Under Voltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200mV.

## Thermal Shutdown

The junction temperature (Tj) of the device is monitored by an internal temperature sensor. If Tj exceeds 160°C (typ), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When Tj decreases below the hysteresis amount, the converter resumes normal operation, beginning with Soft Start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

(1) Maximum allowed voltage is 7V. Therefore, it's recommended to connect it to VOUT, not VIN.

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## APPLICATION INFORMATION

The following information is intended to be a guideline through the individual power supply design process.

### Programming The Output Voltage

While the output voltage of the TPS62130 is adjustable, the TPS62131/2/3 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and may be left floating. It is recommended to connect to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9V to 6V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6 (see Figure 4). It is recommended to choose resistor values which allow a current of at least 2uA, meaning the value of R2 shouldn't exceed 400kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{6}$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin internally to about 7.4V.

### External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6213X is optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see Output Filter And Loop Stability). Table 1 can be used to simplify the output filter component selection.

**Table 1. Recommended LC Output Filter Combinations(1)**

| | 4.7µF | 10µF | 22µF | 47µF | 100µF | 200µF | 400µF |
|---|---|---|---|---|---|---|---|
| 0.47µH | | | | | | | |
| 1µH | | | √ | √ | √ | √ | |
| 2.2µH | | √ | √(2) | √ | √ | √ | |
| 3.3µH | | √ | √ | √ | √ | | |
| 4.7µH | | | | | | | |

(1) The values in the table are nominal values.
(2) This LC combination is the standard value and recommended for most applications.

The TPS6213X can be run with an inductor as low as 1µH. FSW should be set Low in this case. However, for applications running with the low frequency setting (FSW=High) or with low input voltages, 2.2µH is recommended. More detailed information on further LC combinations can be found in SLVA463.

#### Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{7}$$


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$$\Delta I_{L(\max)} = V_{OUT} \cdot \left( \frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right) \quad (8)$$

where

$I_L$(max) is the maximum inductor current,
$\Delta I_L$ is the Peak to Peak Inductor Ripple Current,
L(min) is the minimum effective inductor value and
$f_{SW}$ is the actual PWM Switching Frequency.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6213X and are recommended for use:

**Table 2. List of Inductors**

| Type | Inductance [µH] | Current [A](1) | Dimensions [LxBxH] mm | MANUFACTURER |
|---|---|---|---|---|
| XFL4020-102ME_ | 1.0 µH, ±20% | 4.7 | 4 x 4 x 2.1 | Coilcraft |
| XFL4020-152ME_ | 1.5 µH, ±20% | 4.2 | 4 x 4 x 2.1 | Coilcraft |
| XFL4020-222ME_ | 2.2 µH, ±20% | 3.8 | 4 x 4 x 2.1 | Coilcraft |
| IHLP1212BZ-11 | 1.0 µH, ±20% | 4.5 | 3 x 3.6 x 2 | Vishay |
| IHLP1212BZ-11 | 2.2 µH, ±20% | 3.0 | 3 x 3.6 x 2 | Vishay |
| SRP4020-3R3M | 3.3µH, ±20% | 3.3 | 4.8 x 4 x 2 | Bourns |
| VLC5045T-3R3N | 3.3µH, ±30% | 4.0 | 5 x 5 x 4.5 | TDK |

(1) Lower of $I_{RMS}$ at 40°C rise or $I_{SAT}$ at 30% drop.

The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \quad (9)$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

## Capacitor Selection

### *Output Capacitor*

The recommended value for the output capacitor is 22uF. The architecture of the TPS6213X allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see SLVA463).

Note: In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

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### *Input Capacitor*

For most applications, 10µF will be sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it's required to place a capacitance of 0.1uF from AVIN to AGND, to avoid potential noise coupling. An RC, low-pass filter from PVIN to AVIN may be used but is not required.

### *Soft Start Capacitor*

A capacitance connected between SS/TR pin and AGND allows a user programmable start-up slope of the output voltage. A constant current source supports 2.5µA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \cdot \frac{2.5\mu A}{1.25V} \quad [F] \tag{10}$$

where

$C_{SS}$ is the capacitance (F) required at the SS/TR pin and
$t_{SS}$ is the desired soft-start ramp time (s).

**NOTE**

**DC Bias effect:** High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

### Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50mV and 1.2V, the FB pin will track the SS/TR pin voltage as described in Equation 11 and shown in Figure 39.

$$V_{FB} \approx 0.64 \cdot V_{SS/TR} \tag{11}$$

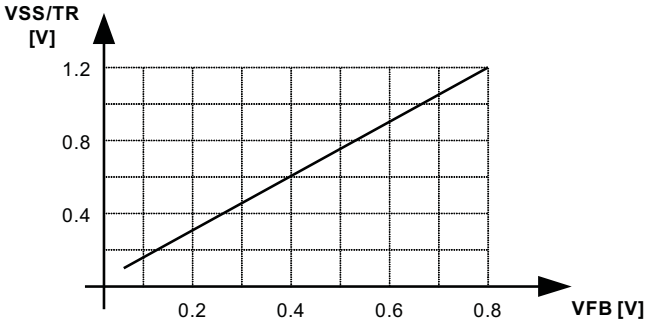



**Figure 39. Voltage Tracking Relationship**


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This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is $V_{IN}$+0.3V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage will go to zero, independent of the tracking voltage. Figure 40 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

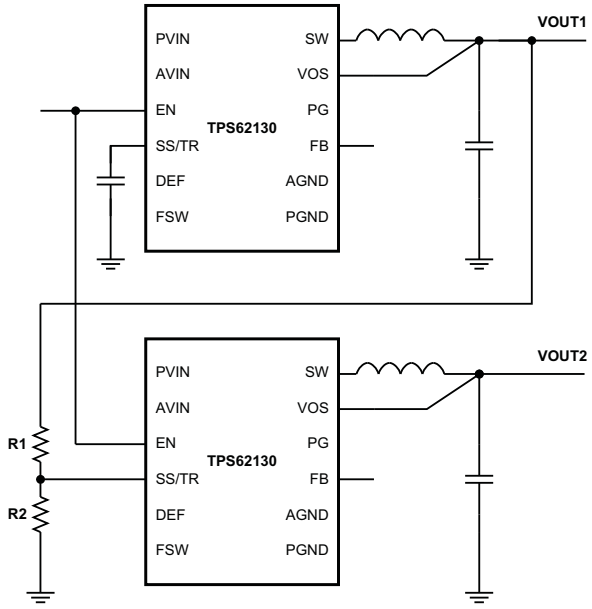



**Figure 40. Sequence for Ratiometric and Simultaneous Startup**

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower or the same as VOUT1.

A sequential startup is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. Ratiometric start up sequence happens if both supplies are sharing the same soft start capacitor. Equation 10 calculates the soft start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in SLVA470.

Note: If the voltage at the FB pin is below its typical value of 0.8V, the output voltage accuracy may have a wider tolerance than specified.

## Output Filter And Loop Stability

The devices of the TPS6213X family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 12:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{12}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 1 and are recommended for use. Different values may work, but care has to be taken on the loop stability which will be affected. More information including a detailed LC stability matrix can be found in SLVA463.

The TPS6213X devices, both fixed and adjustable versions, include an internal 25pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equation Equation 13 and Equation 14:

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$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25pF} \tag{13}$$

$$f_{pole} = \frac{1}{2\pi \cdot 25pF} \cdot \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \tag{14}$$

Though the TPS6213X devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289 and SLVA466.

## Layout Considerations

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6213X demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity.

Provide low inductive and resistive paths for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Also sensitive nodes like FB and VOS should be connected with short wires, not nearby high dv/dt signals (e.g. SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). Signals not assigned to power transmission (e.g. feedback divider, SS/TR capacitor) should refer to the signal ground (AGND) and always be separated from the power ground (PGND).

In summary, the input capacitor should be placed as close as possible to the PVIN and PGND pins of the IC. This connections should be done with wide and short traces. The output capacitor should be placed such that its ground is as close as possible to the IC's PGND pins - avoiding additional voltage drop in traces. This connection should also be made short and wide. The inductor should be placed close to the SW pin and connect directly to the output capacitor - minimizing the loop area between the SW pin, inductor, output capacitor and PGND pin. The feedback resistors, $R_1$ and $R_2$, should be placed close to the IC and connect directly to the AGND and FB pins. Those connections (including VOUT) to the resistors and even more to the VOS pin should stay away from noise sources, such as the inductor. The VOS pin should connect in the shortest way to VOUT at the output capacitor, while the VOUT connection to the feedback divider can connect at the load. The capacitor on the SS/TR pin should be kept close to the IC and its return should be connected to AGND

See Figure 41 for the recommended layout of the TPS6213X. AGND is connected to the Exposed Thermal Pad, which is also connected to PGND and internal metal layers to get best thermal performance. The regulation loop is closed from COUT directly to AGND with vias down to the AGND bottom layer. More detailed information can be found in the EVM Users Guide, SLVU437.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation. Although the Exposed Thermal Pad can be connected to a floating circuit board trace, the device will have better thermal performance if it is connected to a larger ground plane. The Exposed Thermal Pad is electrically connected to AGND.


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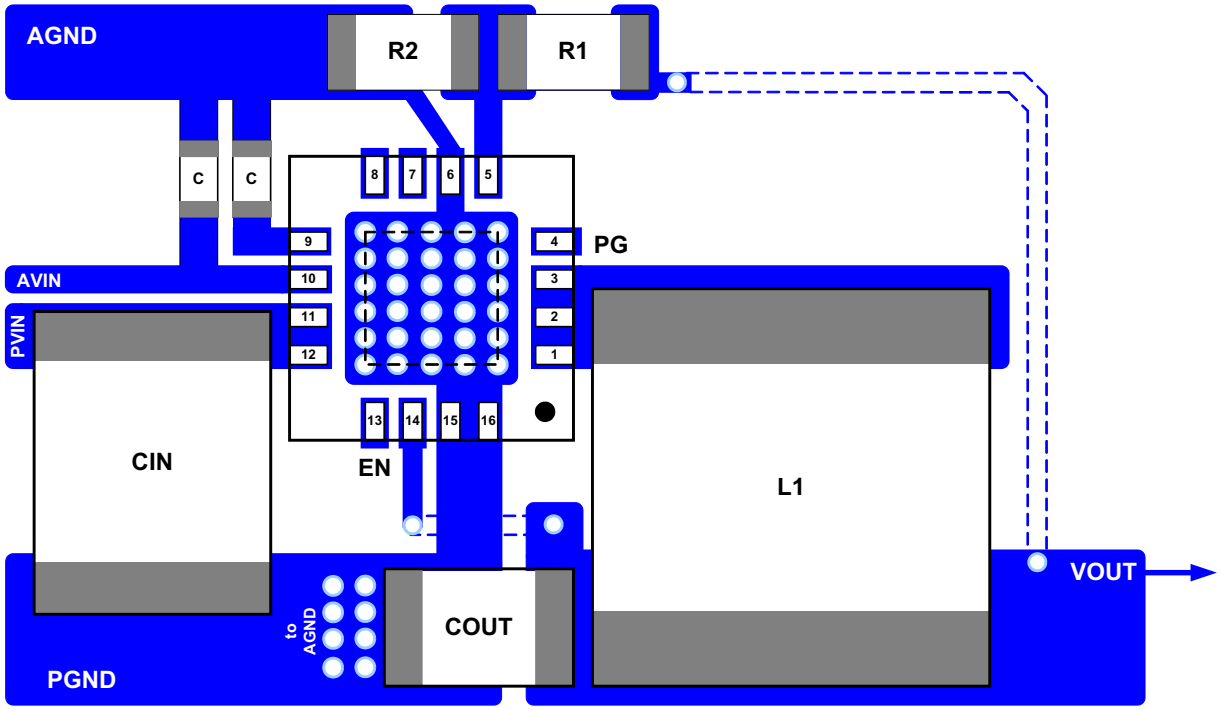



**Figure 41. Layout Example**

## THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (SZZA017), and (SPRA953).

The TPS6213X is designed for a maximum operating junction temperature ($T_j$) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, it's recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation. Experimental data, taken from the TPS62130 EVM, shows the maximum ambient temperature (without additional cooling like airflow or heat sink), that can be allowed to limit the junction temperature to at most 125°C (see Figure 37).

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## Application Example As Power LED Supply

The TPS62130 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Since this pin provides 2.5µA, the feedback pin voltage can be adjusted by an external resistor per Equation 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62130. Figure 42 shows an application circuit, tested with analog dimming:

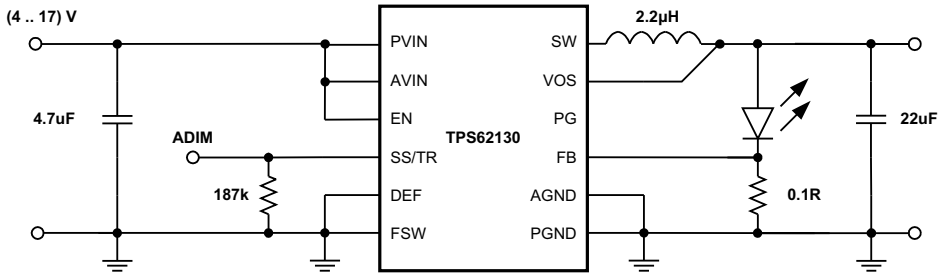



**Figure 42. Single Power LED Supply**

The resistor at SS/TR sets the FB voltage to a level of about 300mV and is calculated from Equation 15.

$$V_{FB} = 0.64 \cdot 2.5\mu A \cdot R_{SS/TR} \quad (15)$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the Application Note SLVA451.

## Typical Applications

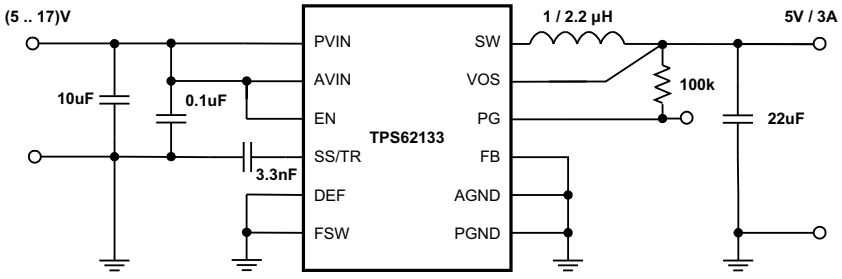



**Figure 43. 5V/3A Power Supply**


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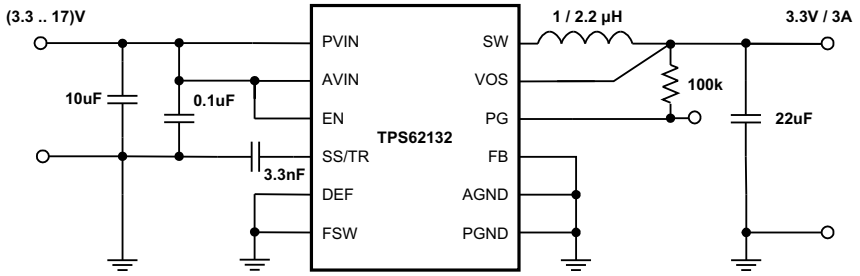



**Figure 44. 3.3V/3A Power Supply**

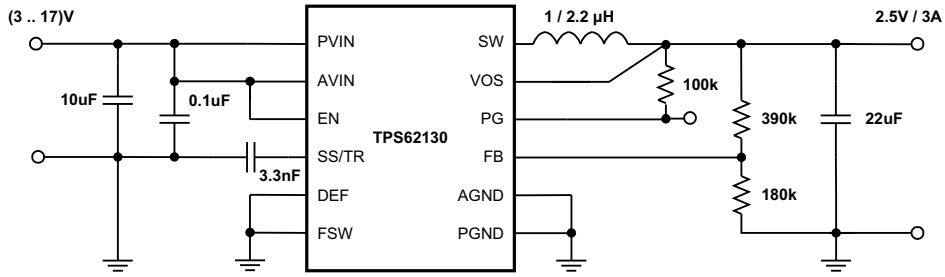



**Figure 45. 2.5V/3A Power Supply**

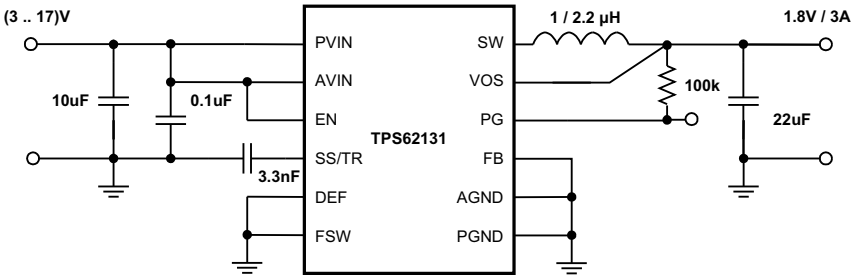



**Figure 46. 1.8V/3A Power Supply**

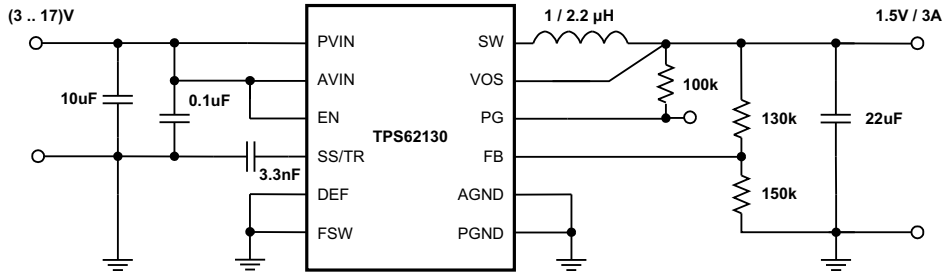



**Figure 47. 1.5V/3A Power Supply**

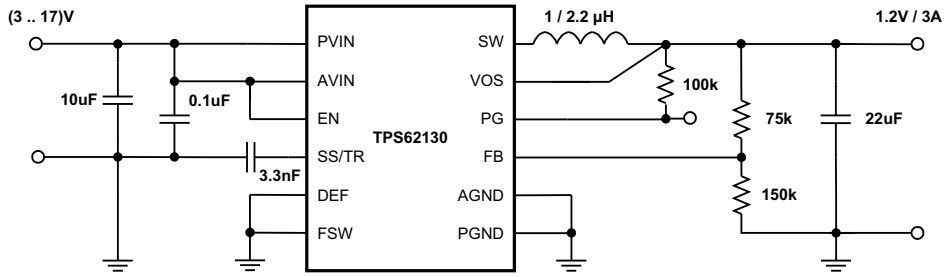



**Figure 48. 1.2V/3A Power Supply**

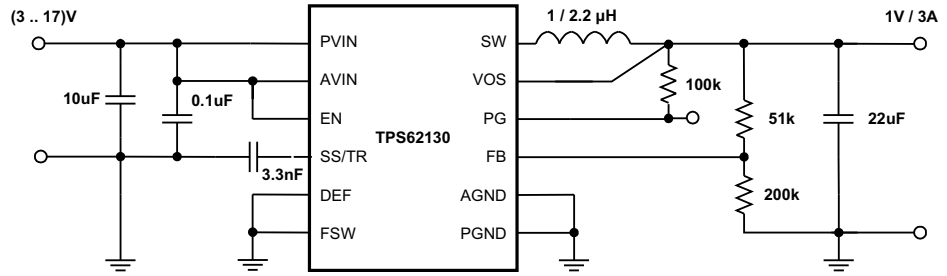



**Figure 49. 1V/3A Power Supply**


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TPS62130RGTR | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS62130RGTT | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS62131RGTR | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS62131RGTT | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS62132RGTR | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS62132RGTT | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS62133RGTR | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS62133RGTT | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

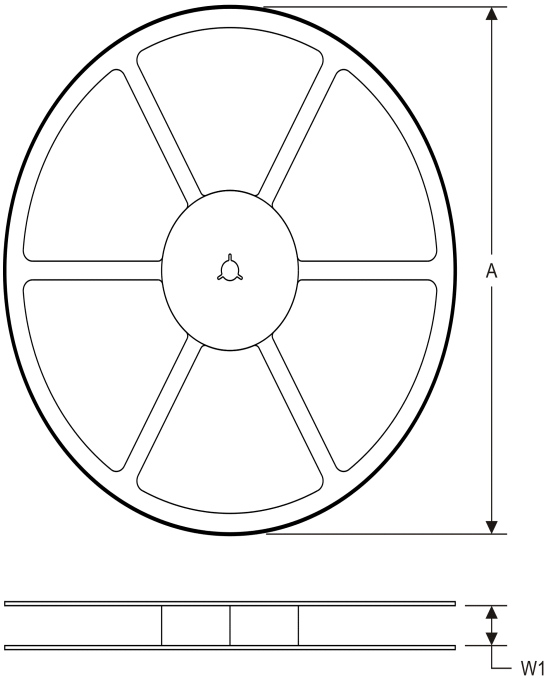
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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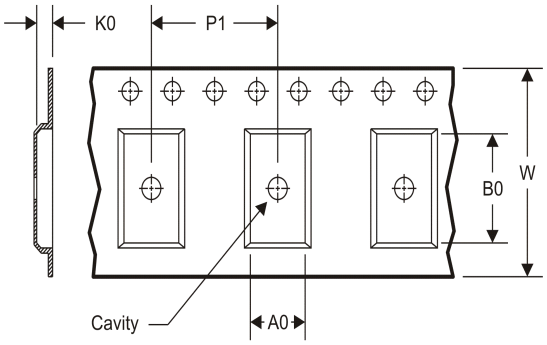
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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



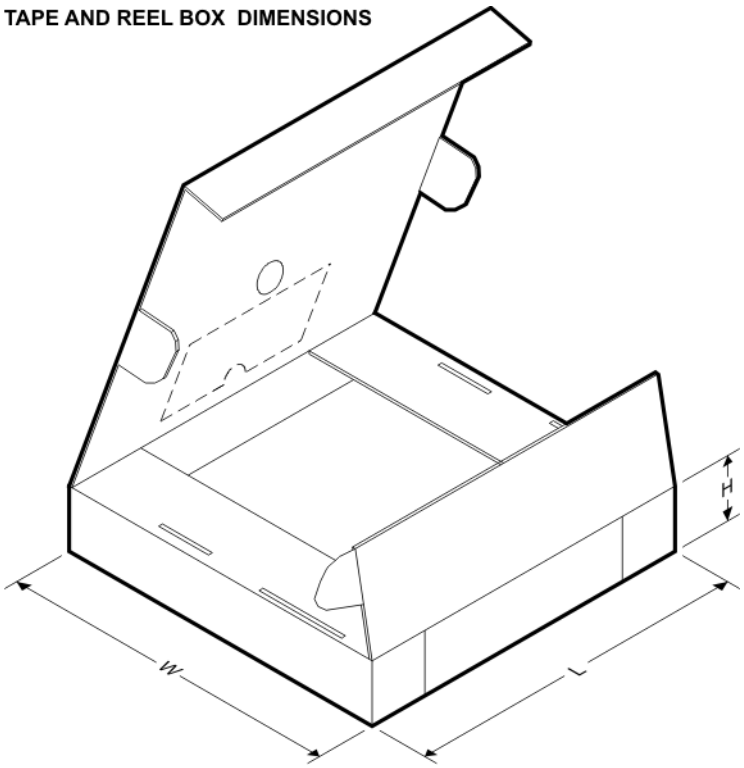

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62130RGTR | QFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS62130RGTT | QFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS62131RGTR | QFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS62131RGTT | QFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS62132RGTR | QFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS62132RGTT | QFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS62133RGTR | QFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS62133RGTT | QFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

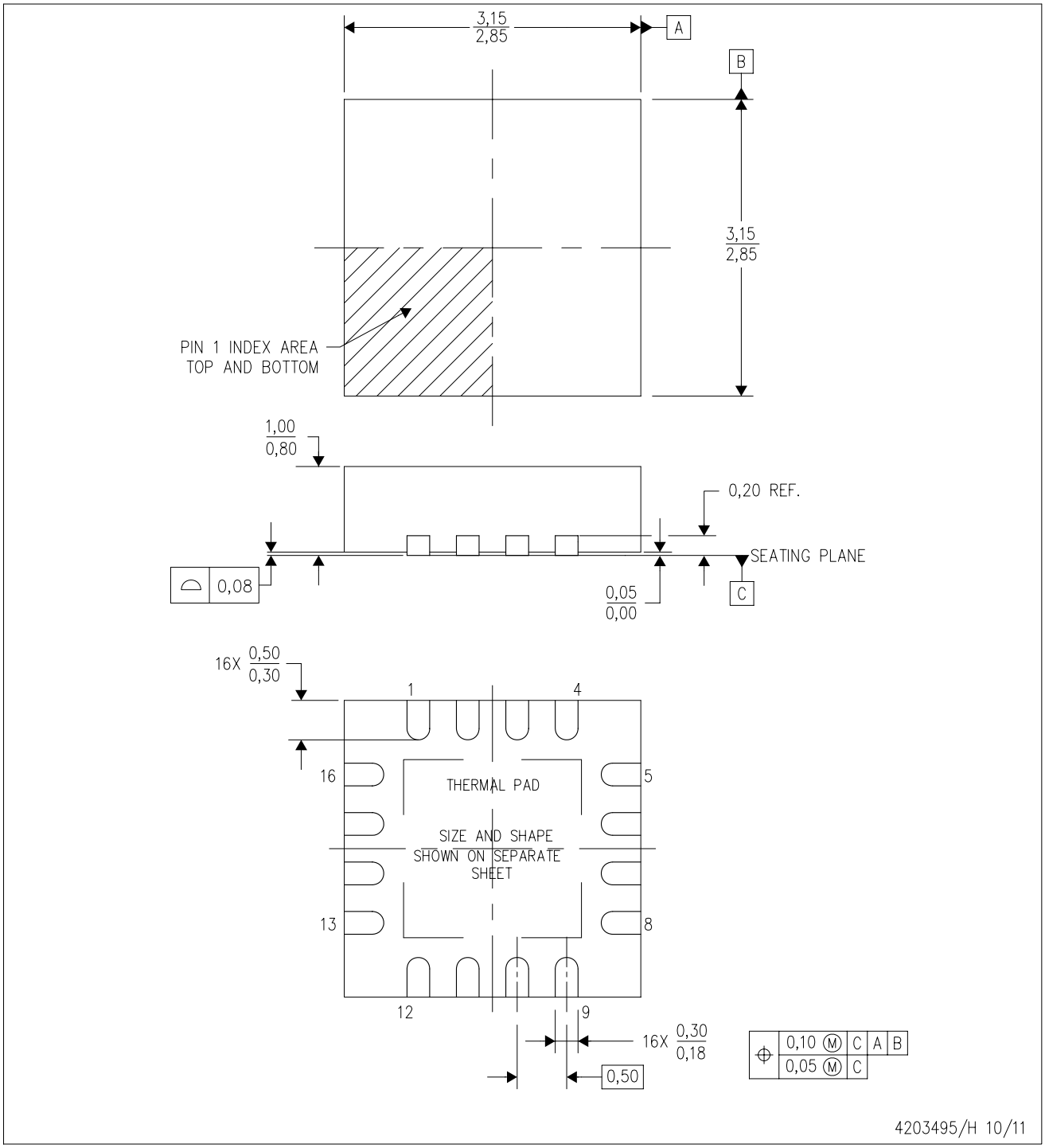
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS62130RGTR | QFN | RGT | 16 | 3000 | 552.0 | 367.0 | 36.0 |
| TPS62130RGTT | QFN | RGT | 16 | 250 | 552.0 | 185.0 | 36.0 |
| TPS62131RGTR | QFN | RGT | 16 | 3000 | 552.0 | 367.0 | 36.0 |
| TPS62131RGTT | QFN | RGT | 16 | 250 | 552.0 | 185.0 | 36.0 |
| TPS62132RGTR | QFN | RGT | 16 | 3000 | 552.0 | 367.0 | 36.0 |
| TPS62132RGTT | QFN | RGT | 16 | 250 | 552.0 | 185.0 | 36.0 |
| TPS62133RGTR | QFN | RGT | 16 | 3000 | 552.0 | 367.0 | 36.0 |
| TPS62133RGTT | QFN | RGT | 16 | 250 | 552.0 | 185.0 | 36.0 |

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

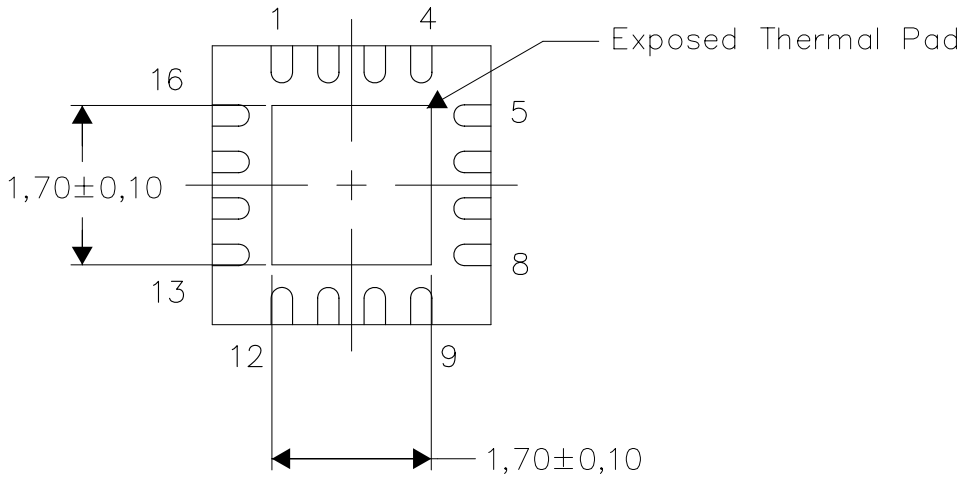
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



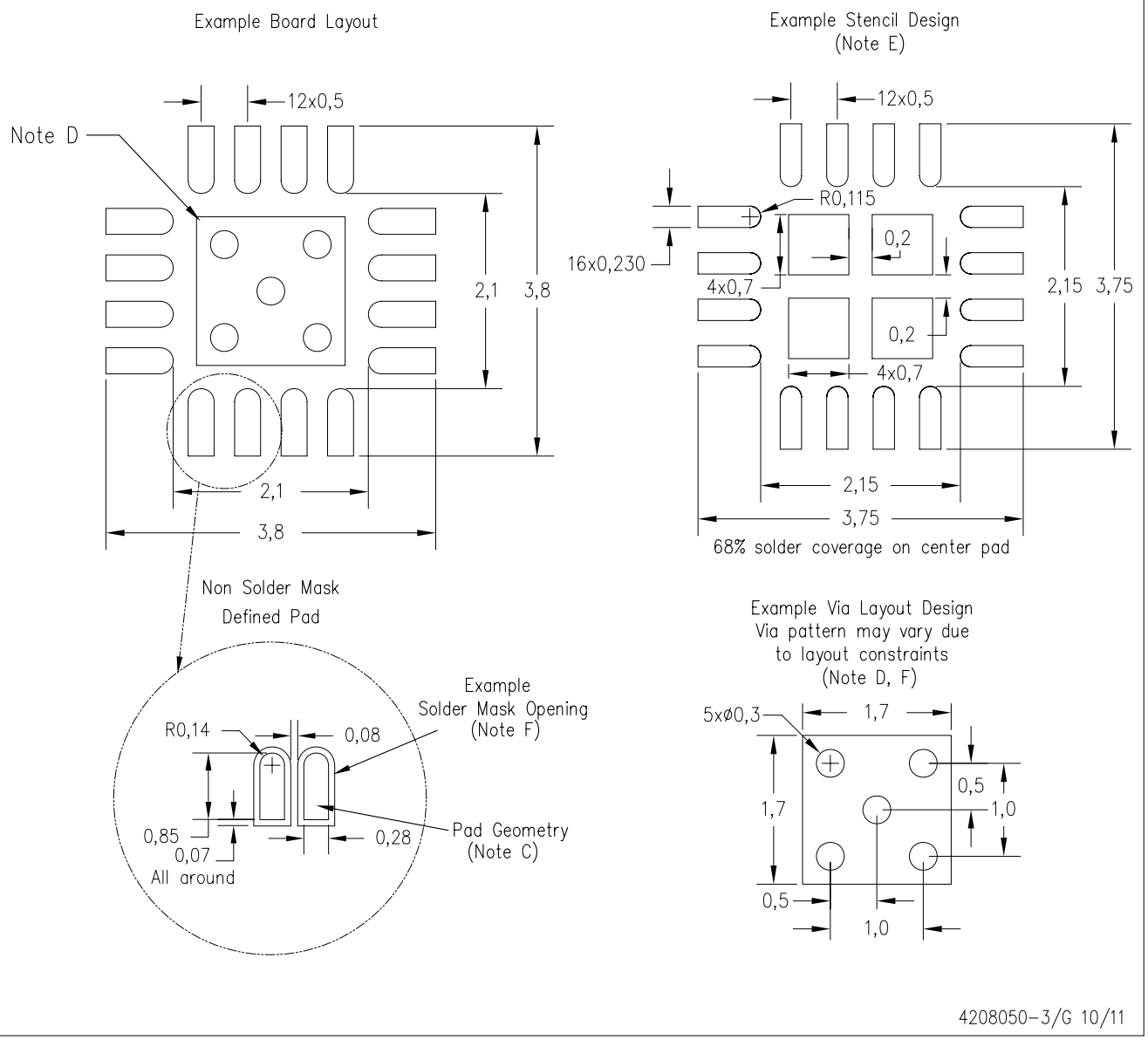

Bottom View

Exposed Thermal Pad Dimensions

4206349–4/Q 10/11

NOTE: All linear dimensions are in millimeters

# RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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