PT7M7803/7809-7812/7823-7825

µP Supervisor Circuits

Features

- Precision supply-voltage monitor
  - 4.63V (PT7M78xxL)
  - 4.38V (PT7M78xxM)
  - 3.08V (PT7M78xxT)
  - 2.93V (PT7M78xxS)
  - 2.63V (PT7M78xxR)
  - 2.32V (PT7M78xxZ)
  - 2.20V (PT7M78xxY)
  - 4.00V (PT7M78xxJ)
  - 2.25V (PT7M78xxK)
  - 2.80V (PT7M78xxG)
- 200ms reset pulse width
- Debounced CMOS-compatible manual-reset input (7811, 7812, 7823, 7825)
- Reset Output Signal for Watchdog and Power Abnormal, Manual Reset
- Reset Push-Pull output (PT7M7809,7811,7823, 7824,7825)
- Reset Open-Drain output (PT7M7803)
- Voltage monitor for power-fail or low battery warning
- Guaranteed $\overline{\text{RESET}}$/RESET valid at V_{CC}=1.0V

Description

The PT7M78xx family microprocessor (µP) supervisory circuits are targeted to improve reliability and accuracy of power-supply circuitry in µP systems. These devices reduce the complexity and number of components required to monitor power-supply and battery functions.

The main functions are:

1. Asserting reset output during power-up, power-down and brownout conditions for µP system.
2. Detecting power failure or low-battery conditions with a 1.25V threshold detector.
3. Watchdog functions
4. Manual reset.

Applications

- Power-supply circuitry in µP systems

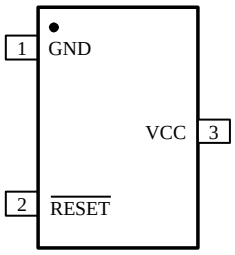
Function Comparison Table

	Part No.	$\overline{\text{RESET}}$ output		RESET output (push-pull)	Manual Reset Input	Power Fail Detector (1.25V)	Watchdog Input
		Push-Pull	Open-Drain				
1	PT7M7803	-	√	-	-	-	-
2	PT7M7809	√	-	-	-	-	-
3	PT7M7810	-	-	√	-	-	-
4	PT7M7811	√	-	-	√	-	-
5	PT7M7812	-	-	√	√	-	-
6	PT7M7823	√	-	-	√	-	√
7	PT7M7824	√	-	√	-	-	√
8	PT7M7825	√	-	√	√	-	-

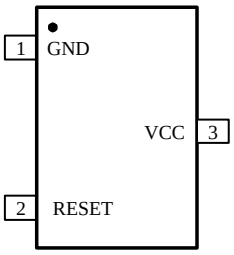
Pin Configuration

SOT23-3

PT7M7803
PT7M7809

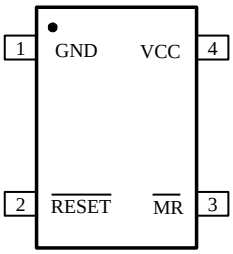


PT7M7810

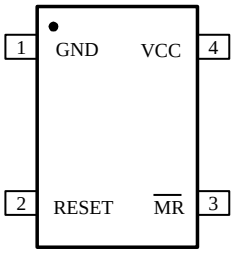


SOT143

PT7M7811

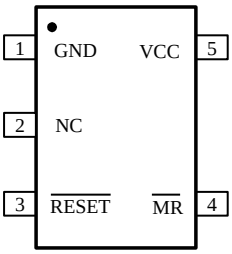


PT7M7812

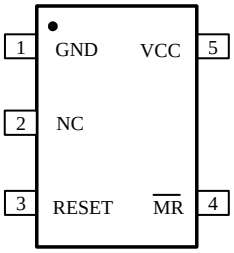


SOT23-5

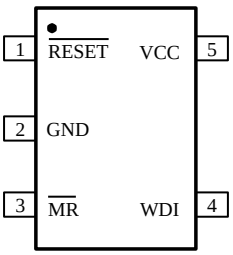
PT7M7811



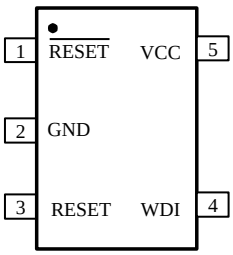
PT7M7812



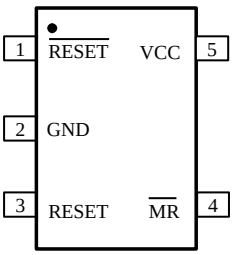
PT7M7823



PT7M7824



PT7M7825

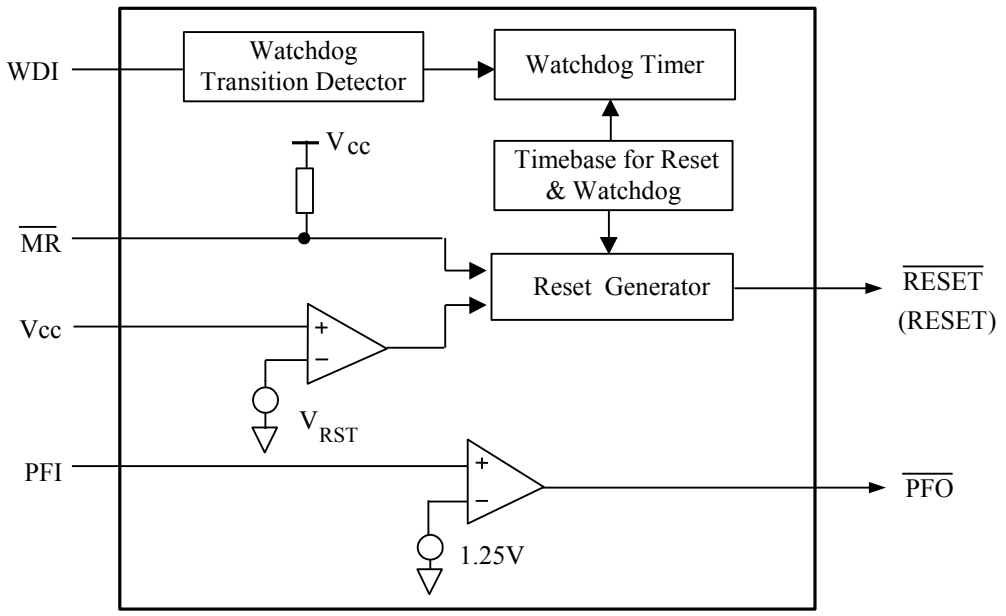


Pin Description

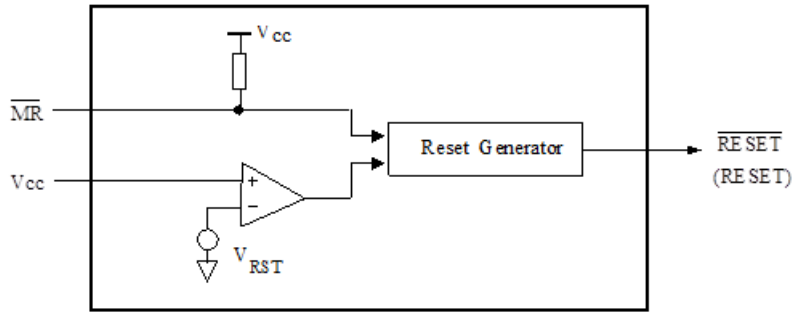
Pin	Type	Description
$\overline{MR}$	I	**Manual-Reset: (CMOS).** Active low. Pull low to force a reset. Reset remains asserted for the duration of the Reset Timeout Period after $\overline{MR}$ transitions from low to high. Leave unconnected or connected to VCC if not used.
VCC	Power	**Supply Voltage.** Reset is asserted when V_{CC} drops below the Reset Threshold Voltage (V_{RST}). Reset remains asserted until V_{CC} rises above V_{RST} and keep asserted for the duration of the Reset Timeout Period (t_{RS}) once V_{CC} rises above V_{RST}.
GND	-	**Ground Reference** for all signals.
PFI	I	**Power-Fail Voltage Monitor Input.** When PFI <V_{PFT}, $\overline{PFO}$ goes low. Connect PFI to GND or Vcc when not used.
$\overline{PFO}$	O	**Power-Fail Output:** it gets low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
WDI	I	**Watchdog Input (CMOS).** If WDI remains high or low for the duration of the watchdog timeout period (t_{WD}), the internal watchdog timer trigger a reset output. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted or WDI occurs a rising or falling edge.
$\overline{RESET}$	O	**Active-Low Reset Output (Push-Pull or Open-Drain).** It goes low when Vcc is below the reset threshold. It remains low for about 200ms after one of the following occurs: Vcc rises above the reset threshold (VRST), the watchdog triggers a reset, or MR goes from low to high.
RESET	O	**The inverse of $\overline{RESET}$,** active high. Whenever $\overline{RESET}$ is high, RESET is low.
NC	-	**No connection.**

Block Diagram

PT7M7823/24/25 Block Diagram



PT7M7811/12 Block Diagram



Maximum Ratings

Storage Temperature .....-65°C to +150°C
Ambient Temperature with Power Applied..... -40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND) .....-0.3V to +7.0V
DC Input Voltage (All inputs except Vcc and GND).....-0.3V to V_{CC}+0.3V
DC Output Current (All outputs) 20mA
Power Dissipation ..... 320mW (Depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage for 78xxL/M/J	-	4.5	5.0	5.5	V
	Supply Voltage for 78xxT/S	-	3.0	3.3	5.5	V
	Supply Voltage for 78xxR/Z/Y/K/G	-	2.7	3.0	5.5	V
V_{IH}	Input High Voltage	-	$0.7V_{CC}$	-	-	V
V_{IL}	Input Low Voltage	-	-	-	$0.3V_{CC}$	V
T_A	Operating Temperature	-	-40	-	85	℃

DC Electrical Characteristics

(V_{CC} = V_{RN} + 5% to 5.5V, T_A= -40~85℃, unless otherwise noted.)(Note 1)

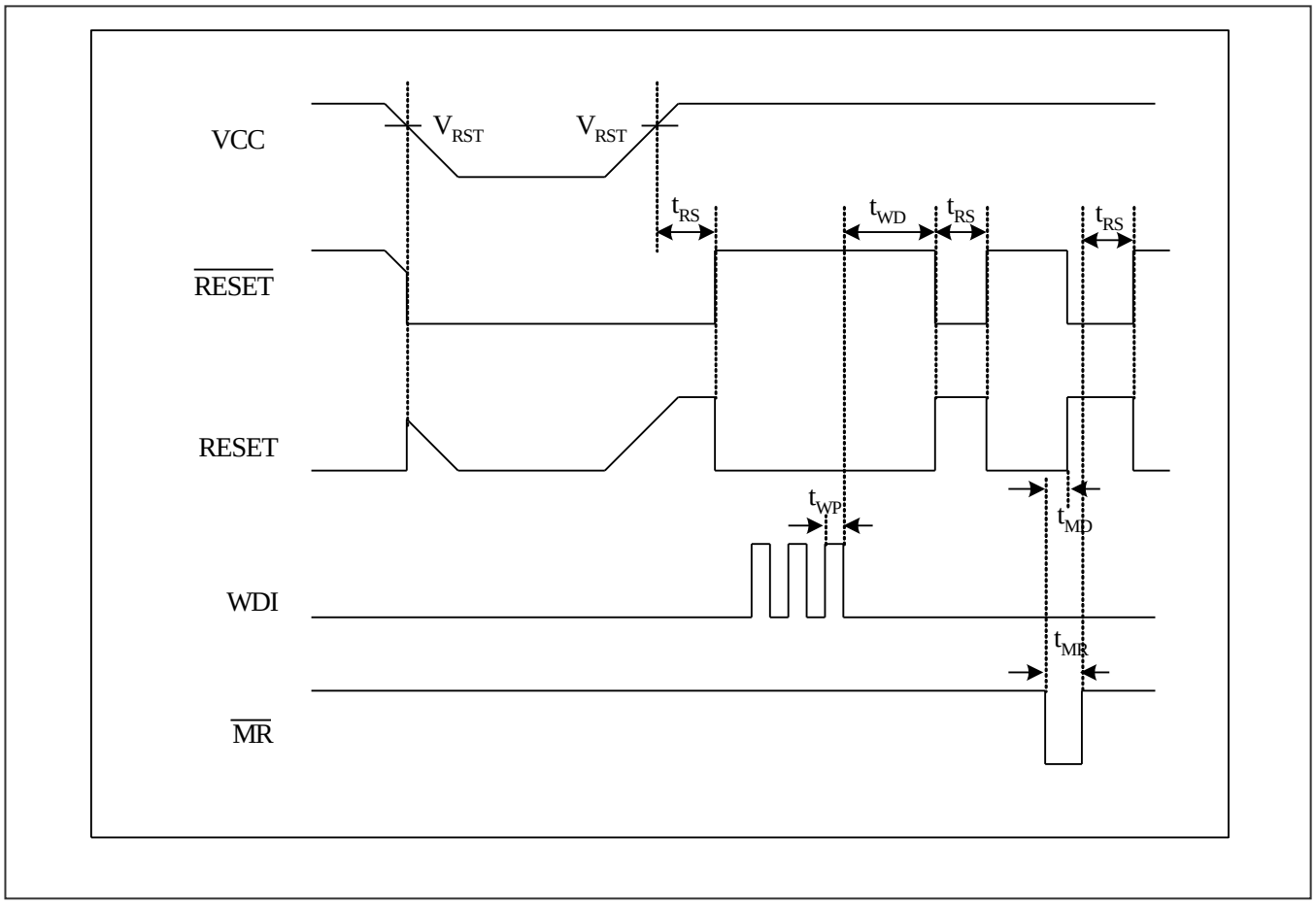
Symbol	Description	Test Conditions		Min	Typ	Max	Unit
V_{CC}	Operating Voltage Range	-		1.0	-	5.5	V
I_{CC}	Supply Current	Vcc = 5V, No load	7803/09/10/11/12	-	10	30	µA
			7823/24/25	-	13	36	
V_{IH}	Input High Voltage	Pin: $\overline{MR}$, WDI		0.7V_{CC}	-	-	V
V_{IL}	Input Low Voltage	Pin: $\overline{MR}$, WDI		-	-	0.3V_{CC}	V
V_{RST}	Threshold Voltage(Falling-edge)(**Note 2**)	T_A= 25℃	78xx	V_{RN} - 1.5%	V_{RN}	V_{RN} + 1.5%	V
		T_A= -40 ~ 85℃		V_{RN} - 2.5%	V_{RN}	V_{RN} + 2.5%	
V_{RTH}	Reset Threshold Hysteresis (**Note 2**)	Vcc varies between V_{RN} ± 5%	7823/24/25L/M	-	12	-	mV
			7823/24/25 T/S/R/K/Z/Y	-	4	-	
			Others	-	50	-	
V_{OH}	Output High Voltage(Except 7823/24/25)	Vcc ≥ 4.5V Isource=800µA		Vcc-1.5	-	-	V
		Vcc ≥ 2.7V Isource=500µA		0.8×Vcc	-	-	
		Vcc ≥ 1.8V Isource=150µA		0.8×Vcc	-	-	
		Vcc ≥ 1.0V Isource=4µA		0.8×Vcc	-	-	
	Output High Voltage(7823/24/25)	7823/24/25L/M, Vcc=V_{RST} Isource=120µA		Vcc-1.5	-	-	V
		7823/24/25T/S/R/K, Vcc=V_{RST} Isource=30µA		0.8×Vcc	-	-	V
V_{OL}	Output Low Voltage	Vcc ≥ 4.5V Isink=3.2mA		-	-	0.4	V
		Vcc ≥ 2.7V Isink=1.2mA		-	-	0.3	
		Vcc ≥ 1.0V Isink=100µA		-	-	0.3	
I_{LKG}	Open-Drain Output Leakage Current	V_{CC} > $V_{TH(MAX)}$ for 7803		-	-	1	µA
I_{WDI}	Average WDI Input Current (**Note 3**)	WDI connected to V_{CC}: 5.5V		-	120	160	µA
		WDI connected to GND		-20	-15	-	
I_{source}	$\overline{RESET}$ Output Short-Circuit Current (only for PT7M7823/24/25)	PT7M782xL/M, $\overline{RESET}$=0V, Vcc=5.5V		-	-	800	µA
		PT7M782xT/S/R/K/Z/Y, $\overline{RESET}$=0V, Vcc=3.6V		-	-	400	
r	MR pull-up resistor (internal)	PT7M7811/7812		10	20	30	kΩ
		PT7M7823/7824/7825		35	52	75	

Note: 1. Parameters of room temperature guaranteed by production test and parameters of full-temperature guaranteed by design.
2. Valid for both $\overline{RESET}$ and RESET. V_{RST} (V_{RTH}-) is the Reset threshold voltage when V_{CC} from high to low level, and V_{RTH}+ is the Reset threshold voltage when V_{CC} from low to high level. V_{RN} is nominal reset threshold voltage.
3. WDI is internally serviced within the watchdog period if WDI is left unconnected.

AC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
t_{RS}	Reset Pulse Width	$\overline{MR}$ from low to High, T_A=25℃	140	200	400	ms
t_{WD}	Watchdog Timeout Period	WDI, $\overline{MR}$ tied to Vcc, Vcc>V_{RN}+5% , T_A=25℃	1.12	1.6	2.25	s
t_{MR}	$\overline{MR}$ Pulse Width	-	200	-	-	ns
t_{MD}	$\overline{MR}$ to $\overline{RESET}$ Delay	Vcc=5V	-	-	250	ns
t_{WP}	WDI Pulse Width	-	150	-	-	ns

Watchdog Timing Diagram



Functional Description

Reset Output

A microprocessor (µP) reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The supervisory circuits assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once Vcc reaches about 1.0V, $\overline{\text{RESET}}$ is a guaranteed logic low of 0.4V or less. As Vcc rises, $\overline{\text{RESET}}$ stays low. When Vcc rises above the reset threshold, an internal timer releases $\overline{\text{RESET}}$ after about 200ms. $\overline{\text{RESET}}$ pulses low whenever Vcc drops below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 200ms. On power-down, once Vcc falls below the reset threshold, $\overline{\text{RESET}}$ stays low and is guaranteed to be 0.4V or less until Vcc drops below 1.0V. Watchdog Timing Diagram shows the timing relationship.

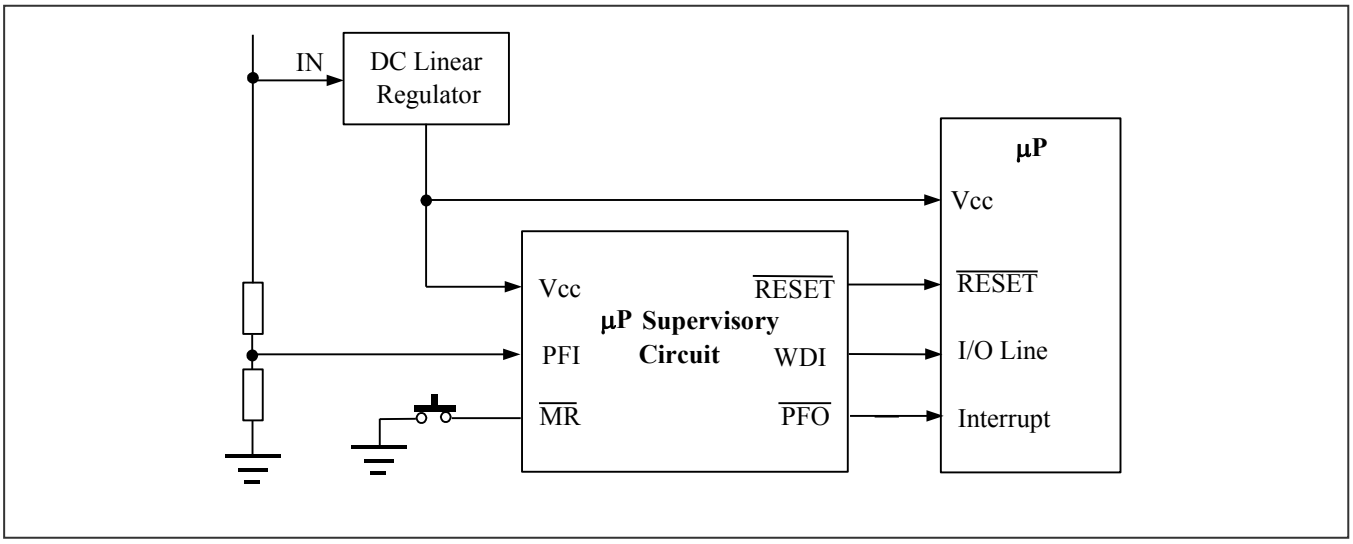
The active-high RESET output is simply the inverse of the $\overline{\text{RESET}}$ output, and is guaranteed to be valid with Vcc down to 1.0V.

Watchdog Timer
The PT7M78xx watchdog circuit monitors the µP activity. If the µP does not toggle the watch-dog input (WDI) within 1.6s, reset asserts. As long as reset is
asserted or the WDI input is toggled, the watchdog timer will stay clear and will not count. As soon as reset is released, the timer will start counting. WDI input pulses as short as 50ns can be detected.
Disable the watchdog function by leaving WDI unconnected or by three-stating driver connected to WDI.

Manual Reset
The manual-reset input ($\overline{\text{MR}}$) allows reset to be triggered by a push button switch. $\overline{\text{MR}}$ has an internal pullup resistor, so it can be left open when not used.

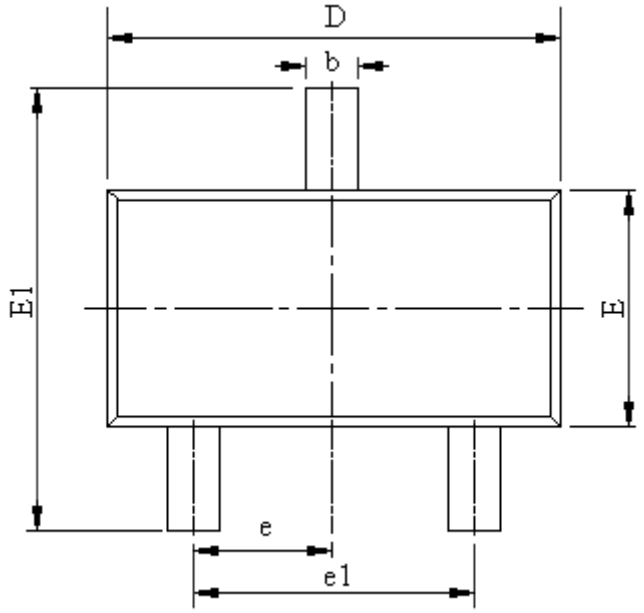
Power-Fail Comparator
The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

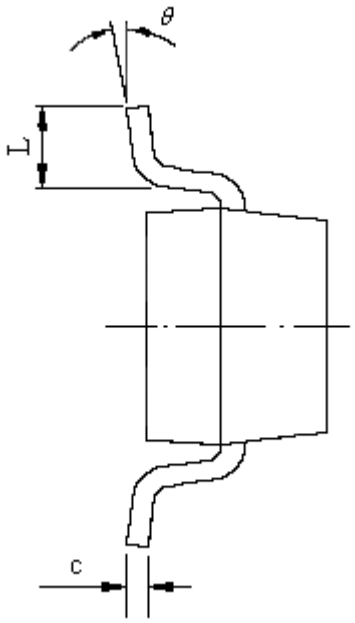
Typical Application Circuit

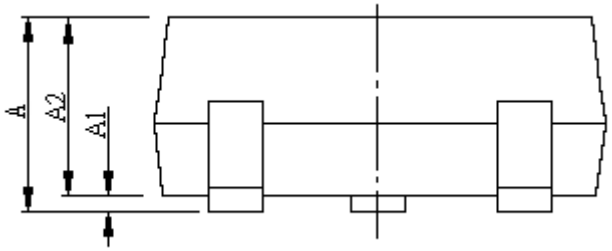


Mechanical Information

TE (SOT23-3)





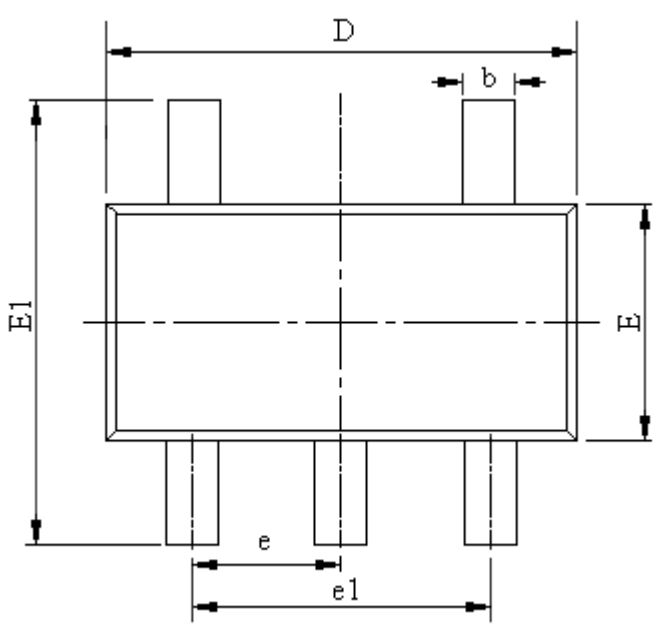


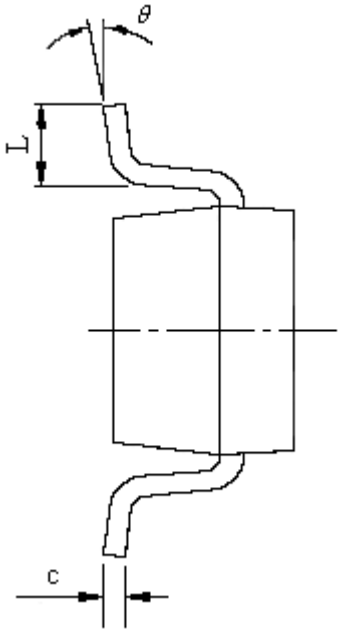
PKG. DIMENSIONS(MM)		
Symbol	Min	Max
A	0.90	1.15
A1	0.00	0.10
A2	0.90	1.05
b	0.30	0.50
c	0.08	0.15
D	2.80	3.00
E	1.20	1.40
E1	2.25	2.55
e	0.95TYP	
e1	1.80	2.00
L	0.30	0.50
θ	0°	8°

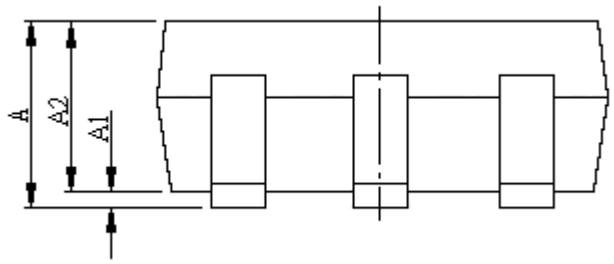
Note:

1) Ref: JEDEC TO-236H;
2) Coplanarity deviation should not exceed 0.1mm

TAE (SOT23-5)



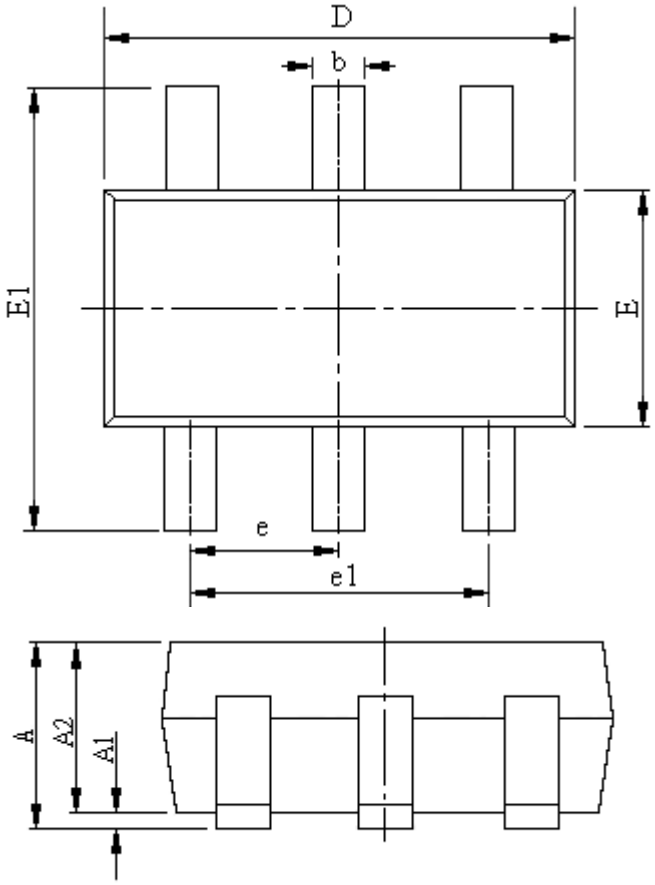


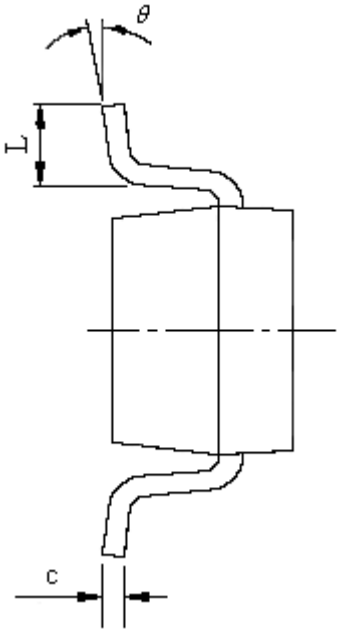


Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MO-178C/AA

PKG. DIMENSIONS(MM)		
SYMBOL	MIN	MAX
A	1.05	1.25
A1	0.00	0.10
A2	1.05	1.15
b	0.30	0.50
c	0.10	0.20
D	2.82	3.02
E	1.50	1.70
E1	2.65	2.95
e	0.95BSC	
e1	1.80	2.00
L	0.30	0.60
θ	0°	8°

TAE (Lead free and Green SOT23-6)

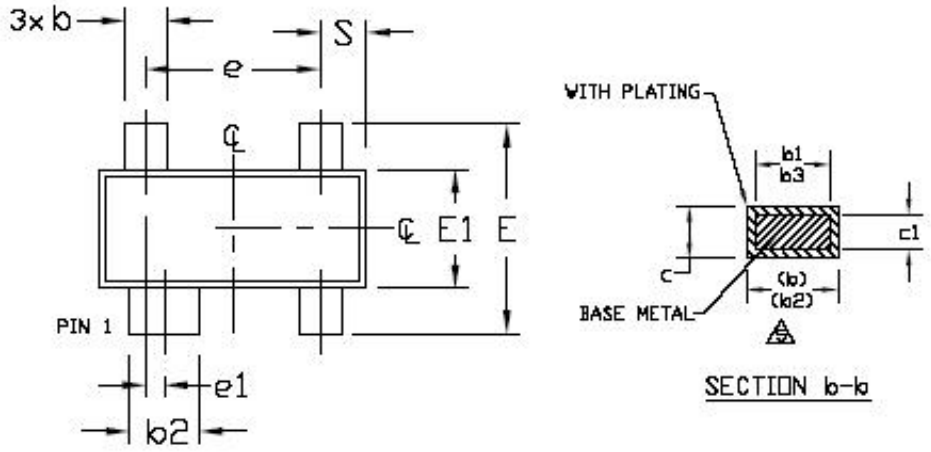


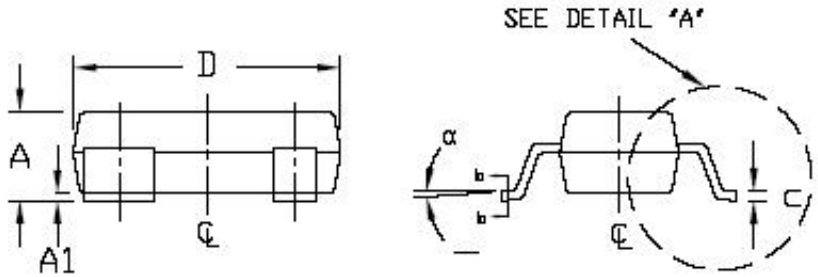


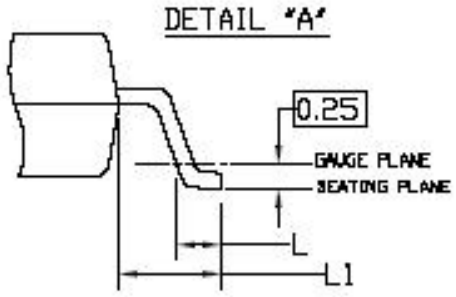
Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MO-178C/AB

PKG. DIMENSIONS(MM)		
SYMBOL	MIN	MAX
A	1.05	1.25
A1	0	0.1
A2	1.05	1.15
b	0.3	0.5
c	0.1	0.2
D	2.82	3.02
E	1.5	1.7
E1	2.65	2.95
e	0.95BSC	
e1	1.8	2
L	0.3	0.6
θ	0°	8°

TBE (Lead free and Green SOT143)







	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.031	0.048	0.80	1.22
A1	0.000	0.006	0.01	0.15
b	0.014	0.020	0.35	0.50
b1	0.012	0.018	0.30	0.45
b2	0.030	0.035	0.76	0.89
b3	0.012	0.033	0.76	0.84
c	0.003	0.008	0.08	0.20
c1	0.003	0.006	0.08	0.16
D	0.110	0.120	2.80	3.04
E	0.083	0.104	2.10	2.64
E1	0.047	0.055	1.20	1.40
e	0.076 BSC.		1.92 BSC.	
e1	0.008 BSC.		0.20 BSC.	
L	0.016	0.024	0.40	0.60
L1	0.021 REF.		0.54 REF.	
S	0.018	0.024	0.45	0.60
α	0°	8°	0°	8°

XX.XX
XX.XX DENOTES DIMENSIONS IN MILLIMETERS

Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC TO-253D

Ordering Information

Part Number	Package Code	Package
PT7M7803XTE	T	Lead free and Green SOT23-3
PT7M7809XTE	T	Lead free and Green SOT23-3
PT7M7810XTE	T	Lead free and Green SOT23-3
PT7M7811XTAE	TA	Lead free and Green SOT23-5
PT7M7812XTAE	TA	Lead free and Green SOT23-5
PT7M7823XTAE	TA	Lead free and Green SOT23-5
PT7M7824XTAE	TA	Lead free and Green SOT23-5
PT7M7825XTAE	TA	Lead free and Green SOT23-5
PT7M7811XTBE	TB	Lead free and Green SOT143
PT7M7812XTBE	TB	Lead free and Green SOT143
PT7M7809XUWF	UWF	Wafer form

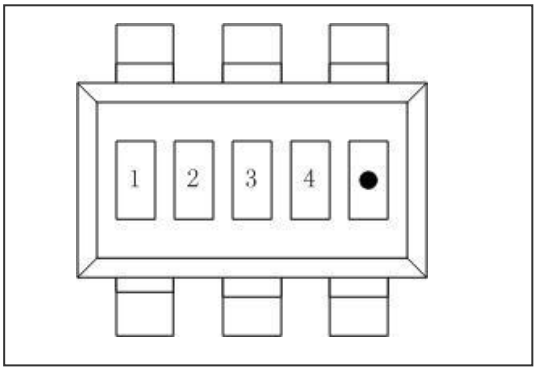
Note:

- "X" refers to voltage range, see below table.
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel
- Contact Pericom for availability.

Suffix: X—Monitored Voltage

X	L	M	T	S	R	Z	Y	J	K	G
Reset Threshold (V)	4.63	4.38	3.08	2.93	2.63	2.32	2.20	4.00	2.25	2.80

Marking Information



Code	Description
1 2	Part Number
3	Year
4	Work Week
●	Only for PT7M7809M

Part Number Code

Code 1 2	Part No	Code 1 2	Part No	Code 1 2	Part No	Code 1 2	Part No
AA	PT7M7809L	AO	PT7M7811L	BC	PT7M7803L	BQ	PT7M7824L
AB	PT7M7809M	AP	PT7M7811M	BD	PT7M7803M	BR	PT7M7824M
AC	PT7M7809T	AQ	PT7M7811T	BE	PT7M7803T	BS	PT7M7824T
AD	PT7M7809S	AR	PT7M7811S	BF	PT7M7803S	BT	PT7M7824S
AE	PT7M7809R	AS	PT7M7811R	BG	PT7M7803R	BU	PT7M7824R
AF	PT7M7809Z	AT	PT7M7811Z	BH	PT7M7803Z	BV	PT7M7824Z
AG	PT7M7809Y	AU	PT7M7811Y	BI	PT7M7803Y	BW	PT7M7824Y
jm	PT7M7809J	sf	PT7M7811J	sc	PT7M7803J	si	PT7M7824J
pE	PT7M7809G					mQ	PT7M7824K
AH	PT7M7810L	AV	PT7M7812L	BJ	PT7M7823L	BX	PT7M7825L
AI	PT7M7810M	AW	PT7M7812M	BK	PT7M7823M	BY	PT7M7825M
AJ	PT7M7810T	AX	PT7M7812T	BL	PT7M7823T	BZ	PT7M7825T
AK	PT7M7810S	AY	PT7M7812S	BM	PT7M7823S	CA	PT7M7825S
AL	PT7M7810R	AZ	PT7M7812R	BN	PT7M7823R	CB	PT7M7825R
AM	PT7M7810Z	BA	PT7M7812Z	BO	PT7M7823Z	CC	PT7M7825Z
AN	PT7M7810Y	BB	PT7M7812Y	BP	PT7M7823Y	CD	PT7M7825Y
se	PT7M7810J	sg	PT7M7812J	sh	PT7M7823J	sj	PT7M7825J
				mP	PT7M7823K		