



SGM8903 Capless 3Vrms Line Driver with Adjustable Gain

GENERAL DESCRIPTION

The SGM8903 is a 3Vrms Pop&Click-less stereo line driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics where size and cost are critical design parameters.

The SGM8903 is capable of driving 3Vrms into a 2.5k Ω load with 5V supply voltage. The device has differential inputs and uses external gain setting resistors, that supports a gain range of $\pm 1V/V$ to $\pm 10V/V$. The use of external gain resistors also allows the implementation of a 2nd order low pass filter to compliment DAC's and SOC converters. The SGM8903 has build-in shutdown control for Pop&Click-free on/off control.

Using the SGM8903 in audio products can reduce component count compared to traditional methods of generating a 3Vrms output. The SGM8903 doesn't require a power supply greater than 5V to generate its 8.5V_{PP} output, nor does it require a split rail power supply. The SGM8903 integrates its own charge pump to generate a negative supply rail that provides a clean, pop&click-less ground biased 3Vrms output.

The SGM8903 is available in a 14 pin TSSOP package. It operates over an ambient temperature range of -40°C to +85°C.

FEATURES

- **Capless Structure**
 - Eliminates Pop/Clicks
 - Eliminates Output DC-Blocking Capacitors
 - Provides Flat Frequency Response DC to 20kHz
- **Low Noise and THD**
 - Typical SNR = 107dB
 - Typical $V_N = 7.5\mu\text{Vrms}$
 - Typical THD+N = 0.001% (f = 1kHz)
- **3Vrms Output Voltage into 2.5k Ω Load with 5V Supply Voltage**
- **Differential Input**

APPLICATIONS

Set-Top Box
LCD TV
Blue-Ray DVD-Players
Home Theater in a Box



PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM8903	TSSOP14	SGM8903YTS14G/TR	SGM8903YTS14	Tape and Reel, 3000

ABSOLUTE MAXIMUM RATINGS

Supply Voltage.....	-0.3V to 6V	Storage Temperature.....	-65°C to +150°C
Input Voltage.....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$	Lead Temperature (soldering, 10s).....	260°C
Minimum load impedance (R_L)	$>600\Omega$	ESD Susceptibility	
EN to GND.....	-0.3V to $V_{DD} + 0.3V$	HBM.....	4000V
Operating Temperature Range.....	-40°C to +85°C	MM.....	400V
Junction Temperature.....	150°C		

NOTE:

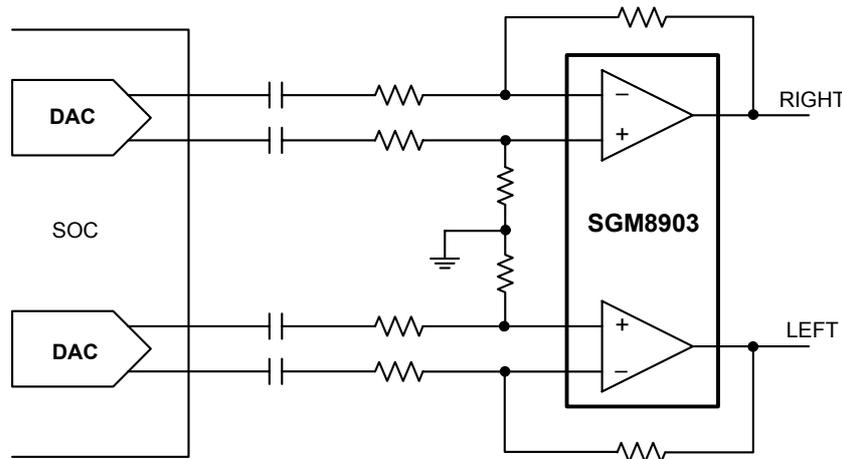
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

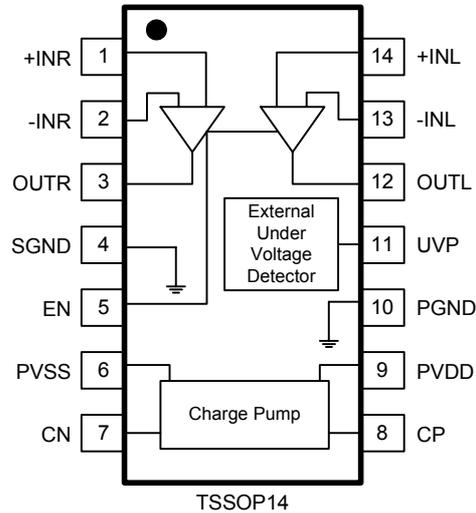
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the last datasheet.

TYPICAL OPERATION CIRCUIT



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	+INR	Right channel OPAMP positive input
2	-INR	Right channel OPAMP negative input
3	OTR	Right channel OPAMP output
4	SGND	Signal ground
5	EN	Enable input, active high
6	PVSS	Negative supply voltage output
7	CN	Charge pump flying capacitor negative terminal
8	CP	Charge pump flying capacitor positive terminal
9	PVDD	Positive supply
10	PGND	Power ground
11	UVP	Undervoltage protection input
12	OUTL	Left channel OPAMP output
13	-INL	Left channel OPAMP negative input
14	+INL	Left channel OPAMP positive input

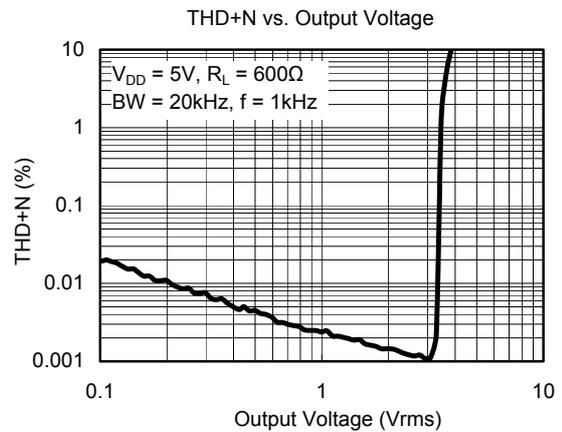
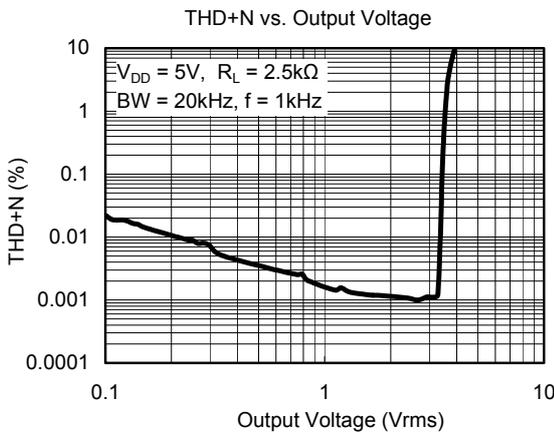
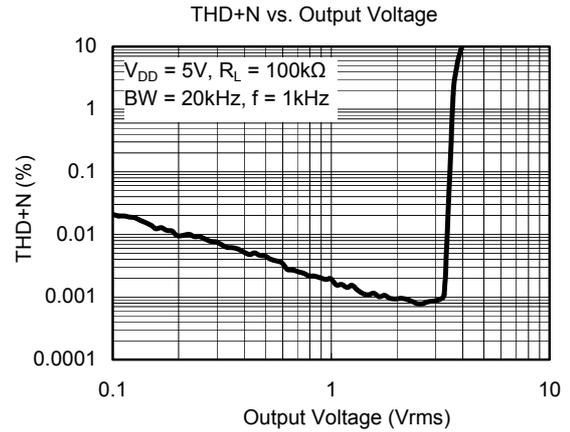
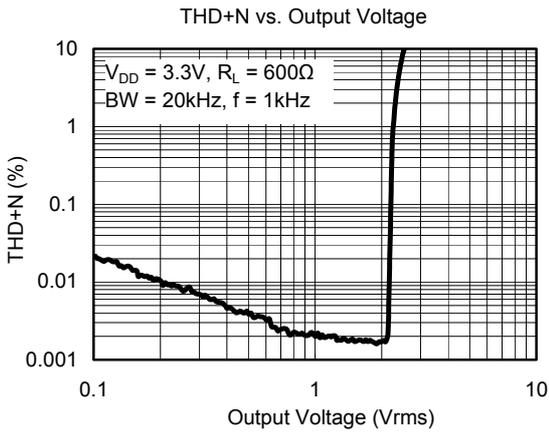
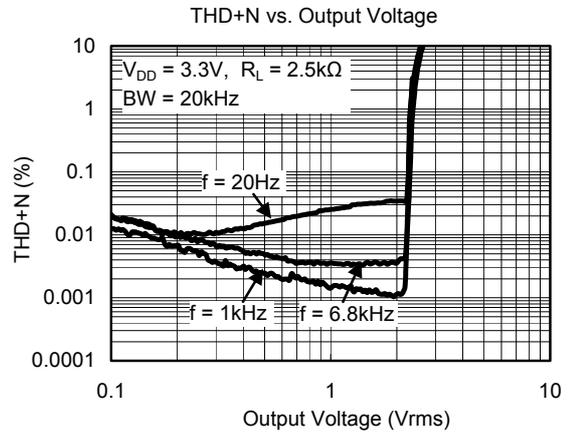
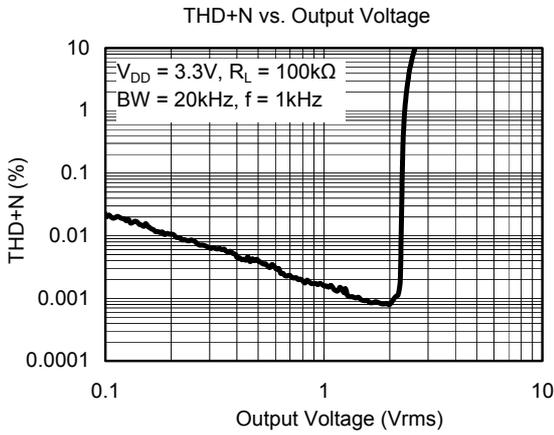
ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ELECTRICAL CHARACTERISTICS					
Output Offset Voltage (V _{OS})	V _{DD} = 3V to 5V		1.2		mV
Supply Rejection Ratio (PSRR)	V _{DD} = 3V to 5V		98		dB
High-Level Output Voltage (V _{OH})	V _{DD} = 3.3V, R _L = 2.5kΩ		3.24		V
Low-Level Output Voltage (V _{OL})	V _{DD} = 3.3V, R _L = 2.5kΩ		-3.16		V
High-Level Input Current (EN) (I _{IH})	V _{DD} = 5V, V _I = V _{DD}			1	μA
Low-Level Input Current (EN) (I _{IL})	V _{DD} = 5V, V _I = 0V			1	μA
Supply Current (I _{DD})	V _{DD} = 3.3V, No load, EN = V _{DD}		10.8		mA
	V _{DD} = 5V, No load, EN = V _{DD}		11.5		
	Shutdown mode, V _{DD} = 3V to 5V		0.11		
OPERATING CHARACTERISTICS (V _{DD} = 3.3V, R _L = 2.5kΩ, C _{I(PUMP)} = C _{I(PVSS)} = 1μF, C _{IN} = 10μF, R _{IN} = 10kΩ, R _{fb} = 20kΩ)					
Output Voltage (Outputs In Phase) (V _O)	THD = 1%, V _{DD} = 3.3V, f = 1kHz		2.3		Vrms
	THD = 1%, V _{DD} = 5V, f = 1kHz		3.53		
	THD = 1%, V _{DD} = 5V, f = 1kHz, R _L = 100kΩ		3.57		
Total Harmonic Distortion Plus Noise (THD+N)	V _O = 2Vrms, f = 1kHz		0.001		%
	V _O = 2Vrms, f = 6.8kHz		0.004		
Crosstalk	V _O = 2Vrms, f = 1kHz		80		dB
Output Current Limit (I _O)	V _{DD} = 3.3V		20		mA
Input Resistor Range (R _{IN})			10		kΩ
Feedback Resistor Range (R _{FB})			20		kΩ
Slew Rate			8		V/μs
Maximum Capacitive Load			220		pF
Noise Output Voltage (V _N)	A-weighted, BW = 20kHz		7.5		μVrms
Signal to Noise Ratio (SNR)	V _O = 3Vrms, THD+N = 0.1%, BW = 20kHz A-weighted		107		dB
Unity Gain Bandwidth (G _{BW})			5.4		MHz
Open-Loop Voltage Gain (A _{VO})			120		dB
Charge Pump Frequency (F _{CP})			407		kHz
External Undervoltage Detection (V _{UVP})			1.15		V
External Undervoltage Detection Hysteresis Current (I _{HYS})			4.4		μA
SHUTDOWN PIN					
Input High Voltage (V _{INH})		1.1			V
Input Low Voltage (V _{INL})				0.6	V
RECOMMENDED OPERATING CONDITIONS					
DC Supply Voltage (V _{DD})		3		5.5	V

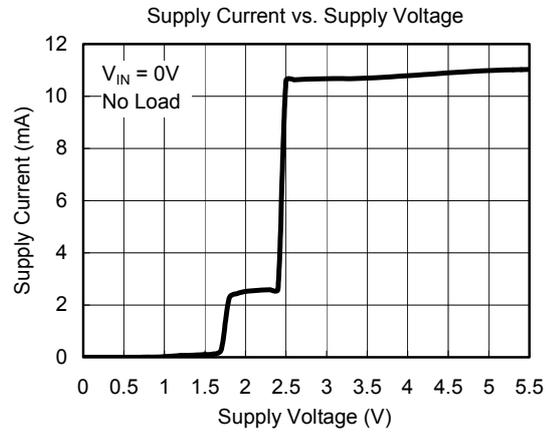
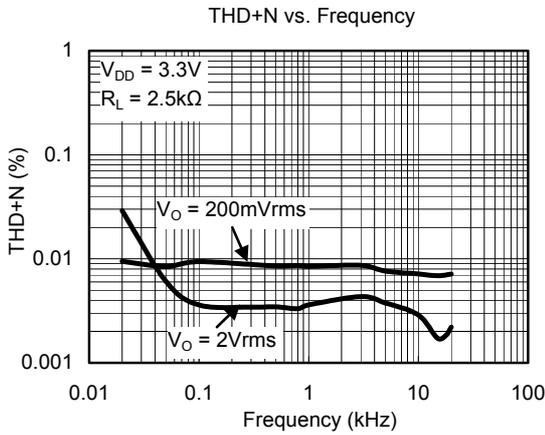
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 3.3V$, $T_A = 25^\circ C$, $R_L = 2.5k\Omega$, $C_{(PUMP)} = C_{(PVSS)} = 1\mu F$, $C_{IN} = 10\mu F$, $R_{IN} = 10k\Omega$, $R_{FB} = 20k\Omega$ (unless otherwise noted).

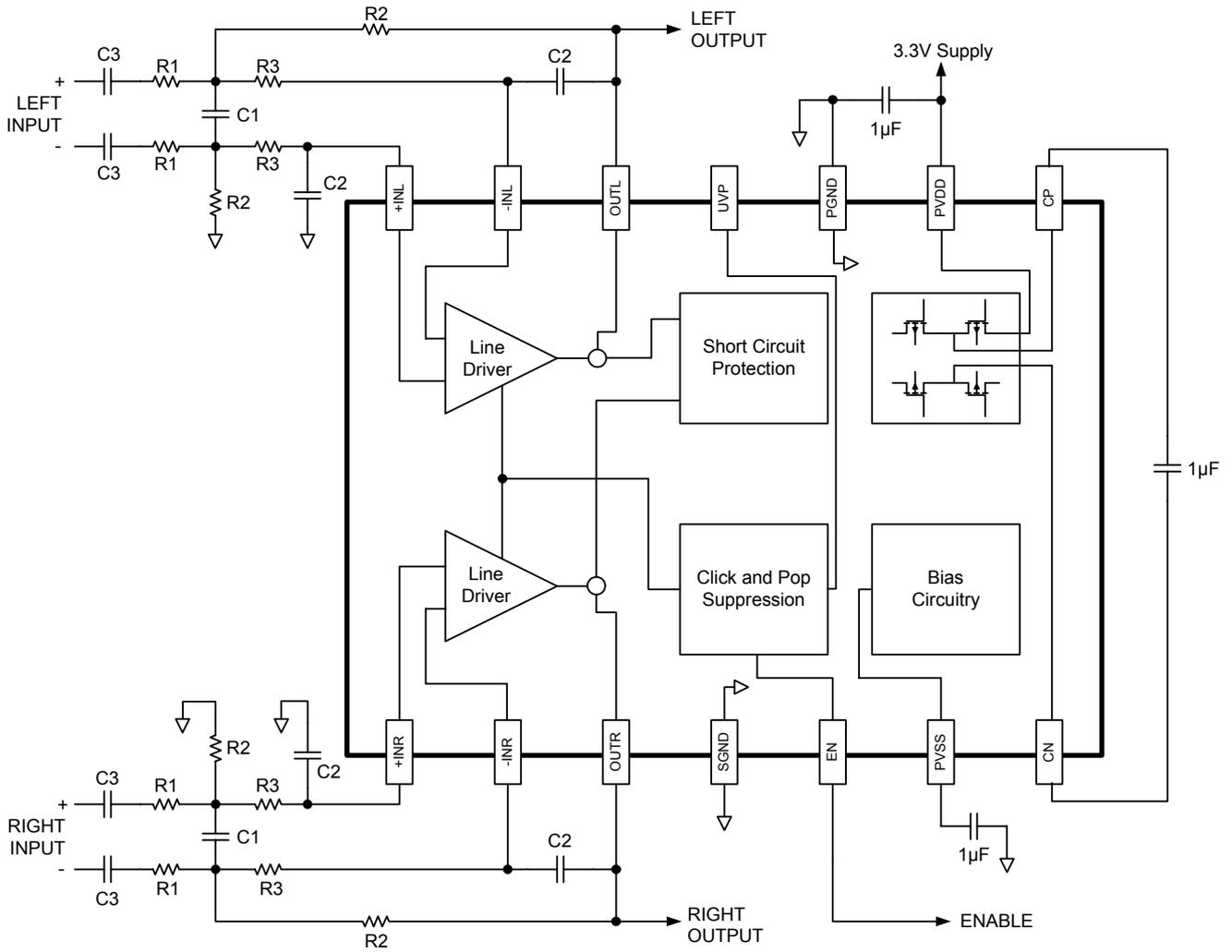


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APPLICATION CIRCUIT



APPLICATION INFORMATION

Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1µF is typical. Capacitor values that are smaller than 1µF can be used, but the maximum output voltage may be reduced and the device may not operate to specifications.

Decoupling Capacitors

The SGM8903 is a capless Line Driver amplifier that require adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the SGM8903 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Gain Setting Resistors Ranges

The gain setting resistors, R_{IN} and R_{fb}, must be chosen so that noise, stability and input capacitor size of the SGM8903 is kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{IN}.

Selecting values that are too low demands a large input ac-coupling capacitor, C_{IN}. Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different gain settings.

Table 1. Recommended Resistor Values

INPUT RESISTOR VALUE, R _{IN}	FEEDBACK RESISTOR VALUE, R _{FB}	DIFFERENTIAL INPUT GAIN	INVERTING INPUT GAIN	NON INVERTING INPUT GAIN
22kΩ	22kΩ	1.0V/V	-1.0V/V	2.0V/V
15kΩ	30kΩ	1.5V/V	-1.5V/V	2.5V/V
33kΩ	68kΩ	2.1V/V	-2.1V/V	3.1V/V
10kΩ	100kΩ	10.0V/V	-10.0V/V	11.0V/V

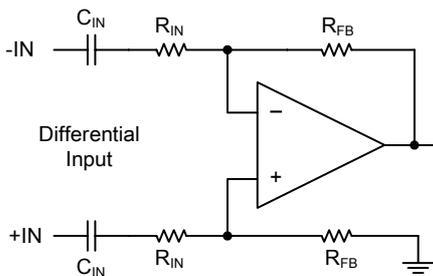


Figure 1. Differential Input

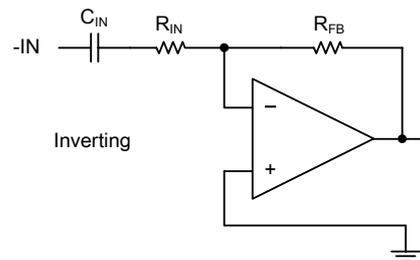


Figure 2. Inverting

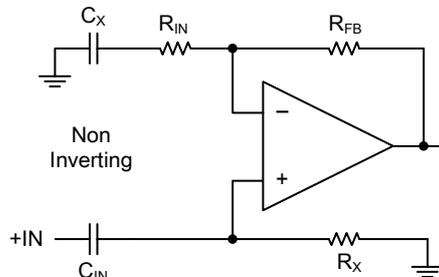


Figure 3. Non-Inverting

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the SGM8903. These capacitors block the DC portion of the audio source and allow the SGM8903 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC gain to 1, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN} . The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1, then the frequency and/or capacitance can be determined when one of the two values are given.

$$f_{c_{IN}} = \frac{1}{2\pi R_{IN} C_{IN}} \text{ or } C_{IN} = \frac{1}{2\pi f_{c_{IN}} R_{IN}} \quad (1)$$

Using the SGM8903 as 2nd Order Filter

Several audio DACs used today require an external low-pass filter to remove out of band noise. This is possible with the SGM8903 as it can be used like a standard OPAMP.

Several filter topologies can be implemented both single ended and differential. In Figure 4, a Multi Feedback-MFB, with differential input and single ended input is shown.

An ac-coupling capacitor to remove dc-content from the source is shown, it serves to block any dc content from the source and lowers the dc-gain to 1 helping reducing the output dc-offset to minimum.

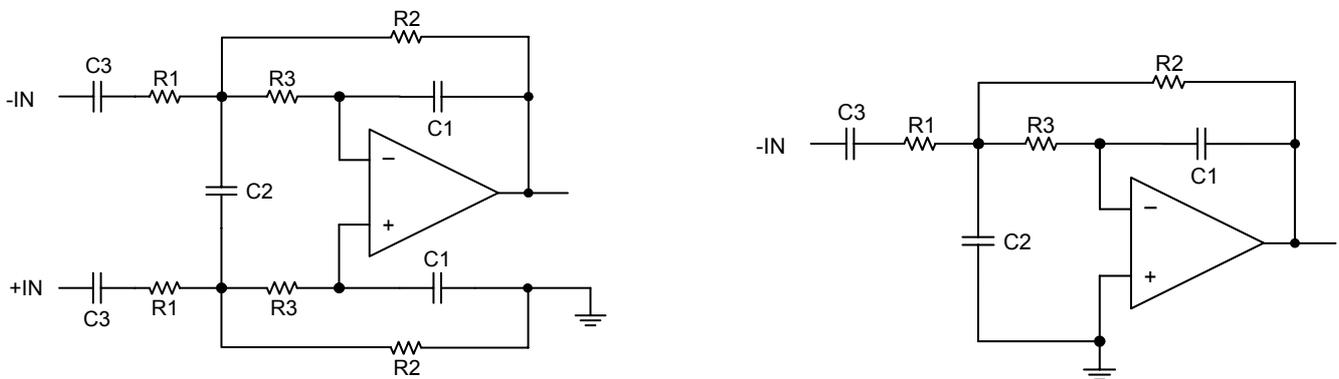


Figure 4. 2nd Order Active Low Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling cap. Using 5.6 kΩ for the resistors, C1 = 220pF, and C2 = 470pF, a SNR of 107dB can be achieved with a 10μF input ac-coupling capacitor.

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{SD(EN)}$ (shutdown pin) low during power supply ramp up and down. The EN pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the EN pin high, this way proper precharge of the ac-coupling is performed, and pop-less power-up is achieved. Figure 5 illustrates the preferred sequence.

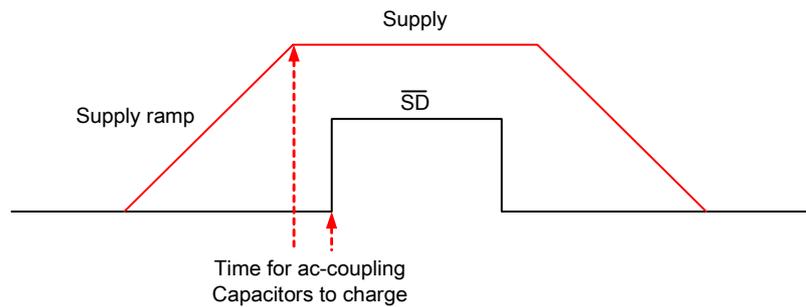


Figure 5. Power-Up Sequence

External Undervoltage Detection

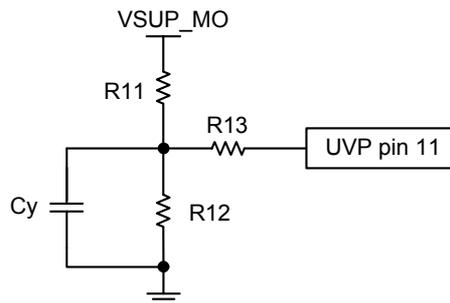
External undervoltage detection can be used to mute/shut down the SGM8903 before an input device can generate a pop.

The shutdown threshold at the UVP pin is 1.15 V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application. The thresholds can be determined as follows:

$$V_{\text{UVP}} = 1.15 \text{ V} \times (R11 + R12) / R12$$

$$\text{Hysteresis} = 4.4 \mu\text{A} \times R13 \times (R11 + R12) / R12$$

with the condition $R13 \gg R11/R12$.



Capacitive Load

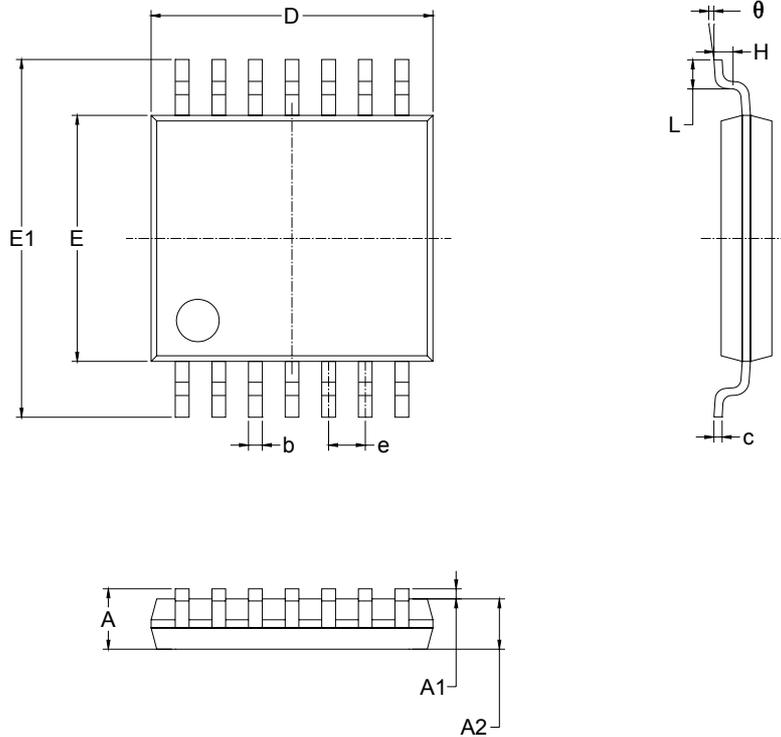
The SGM8903 has the ability to drive a high capacitive load up to 220pF directly, higher capacitive loads can be accepted by adding a series resistor of 47Ω or larger.

Gain-Setting Resistors

The gain setting resistors, R_{IN} and R_{FB} , must be placed close to the input pins to minimize the capacitive loading on these input pins and to ensure maximum stability of the SGM8903.

PACKAGE OUTLINE DIMENSIONS

TSSOP14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

Important Note:

This preliminary data sheet is provided to assist you in the evaluation of engineering samples of the product. It is not intended to be complete or correct in any detail. There might be major changes for the final version.

