AU6259-JBF

USB2.0 Hub Controller

Technical Reference Manual

Rev. 1.03

Aug, 2012

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Revision History

Date	Revision	Description
May 2011	1.00	Official Release
June 2011	1.01	Modify Table 3.1 28 QFN Pin Descriptions
Sep 2011	1.02	Modify 1.2 Feature, Table 3.1 Pin Descriptions, and Adding 5.7 Power Consumption Note.
Aug 2012	1.03	Modify Table 6.2 Recommended Operating Conditions.

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1. Introduction

1.1 Description

AU6259 is a fully compliant with the USB 2.0 hub specification and is designed to work with USB host as a high-speed hub. Its built-in TT (Transaction Translator) allows system to benefit combinational performance under the unbalanced traffic condition.

AU6259-JBF supports two USB downstream ports and one upstream port in 28QFN package. Each downstream port could be a device of high-speed, full-speed or low-speed traffic, while the upstream port supports both high-speed and full-speed traffic. For each downstream port it has individual power switch control built-in as over-current sensing control.

In addition to the application as a stand-alone hub, AU6259 is also very suitable for usage in notebook and motherboard design to provide additional USB ports. All these product advantages should be attributed to its compliance to standards, performance and low power consumption.

1.2 Features

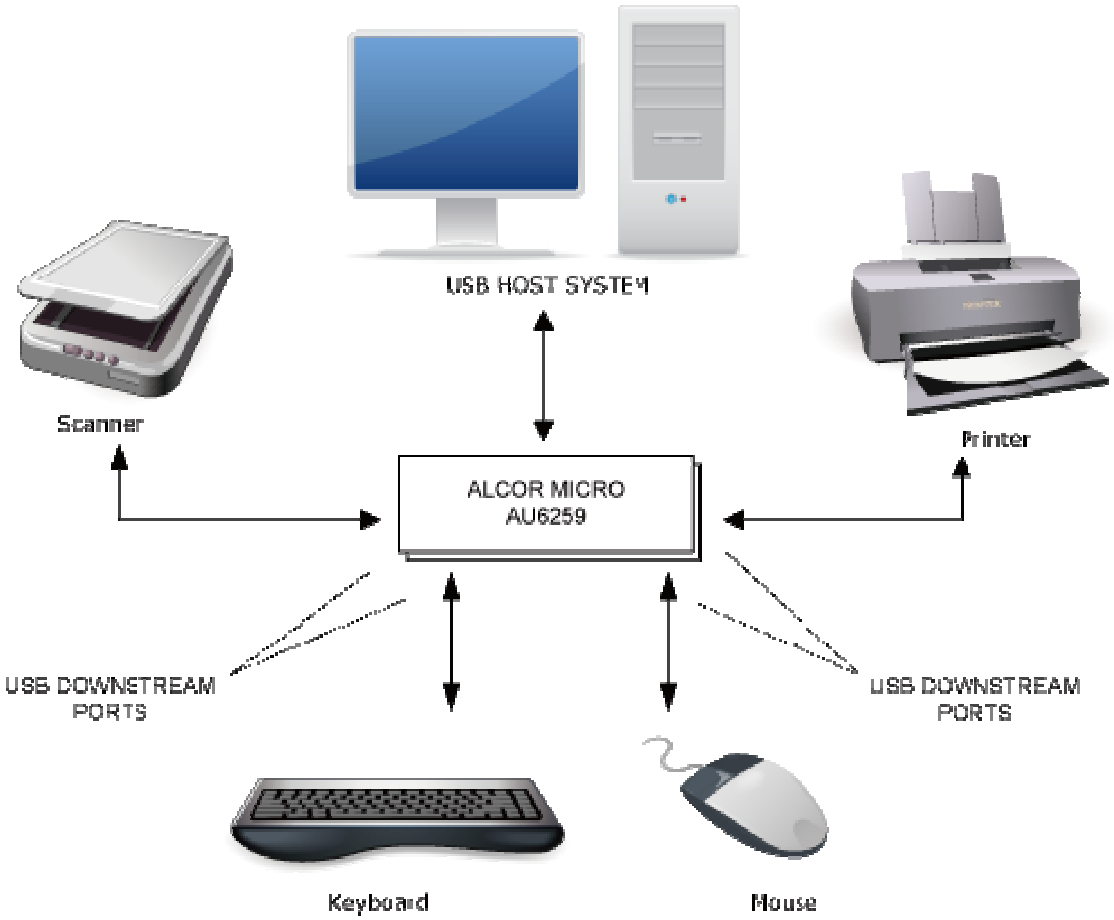
- Fully compliant with USB Hub Specification version 2.0 and is also backward
- compatible with USB Hub specification 1.1.
- Support the Charging Downstream Port of USB Battery Charging specification, V1.2.
- Single chip USB 2.0 hub controller.
- Supports two bus-powered/self-powered downstream ports.
- Supports automatic switching between bus- and self-powered modes.
- Cost effective design using one transaction translator for all downstream ports.
- Suspend LED controls is available to indicate the status of Hub.
- Extra low power consumption.
- Built-in 15K pull-down resistors for all data lines of downstream ports.
- Built-in USB 2.0 transceiver.
- Supports gang mode of power management.

- Built-in power enabling control and over current sensing control for power switch application.
- Built-in 5V to 3.3V and 3.3V to1.8V regulator for core logic.
- Embedded in PLL (Phase Lock Loop) circuit for 12MHz operation precision
- Available in 28-pin QFN package

2. Application Block Diagram

AU6259-JBF is a single chip 2-ports USB hub controller. Its upstream port is connected to a USB Host system. The downstream ports can be used for a mouse, joystick, scanner, printer or other devices.

Figure 2.1 Block Diagram



3. Pin Assignment

AU6259-JBF is in 28-pin QFN package. Below diagram shows signal name of each pin and table in the following page describes each pin in detail.

Figure 3.1 AU6259-JBF Pin Assignment Diagram

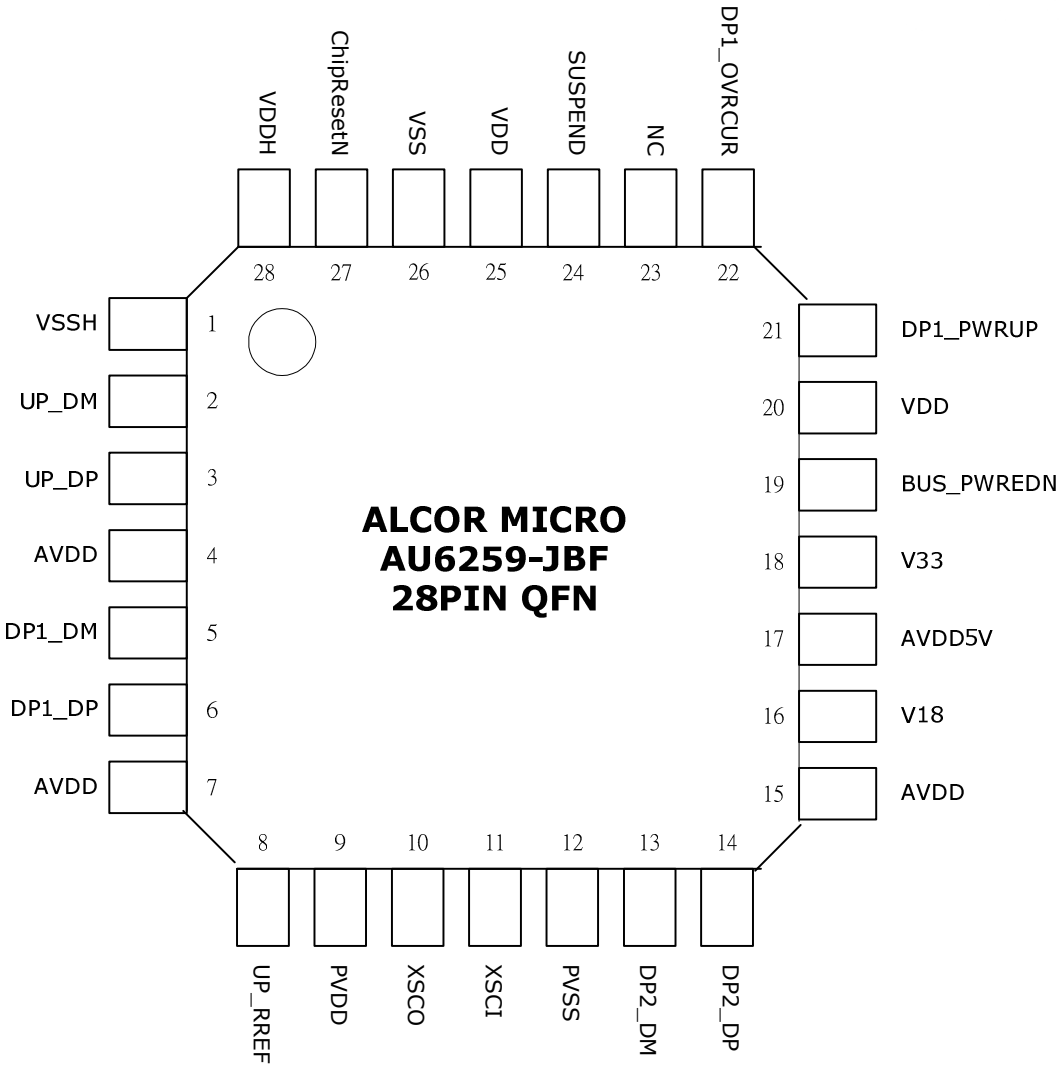


Table 3.1 AU6259-JBF Pin Descriptions

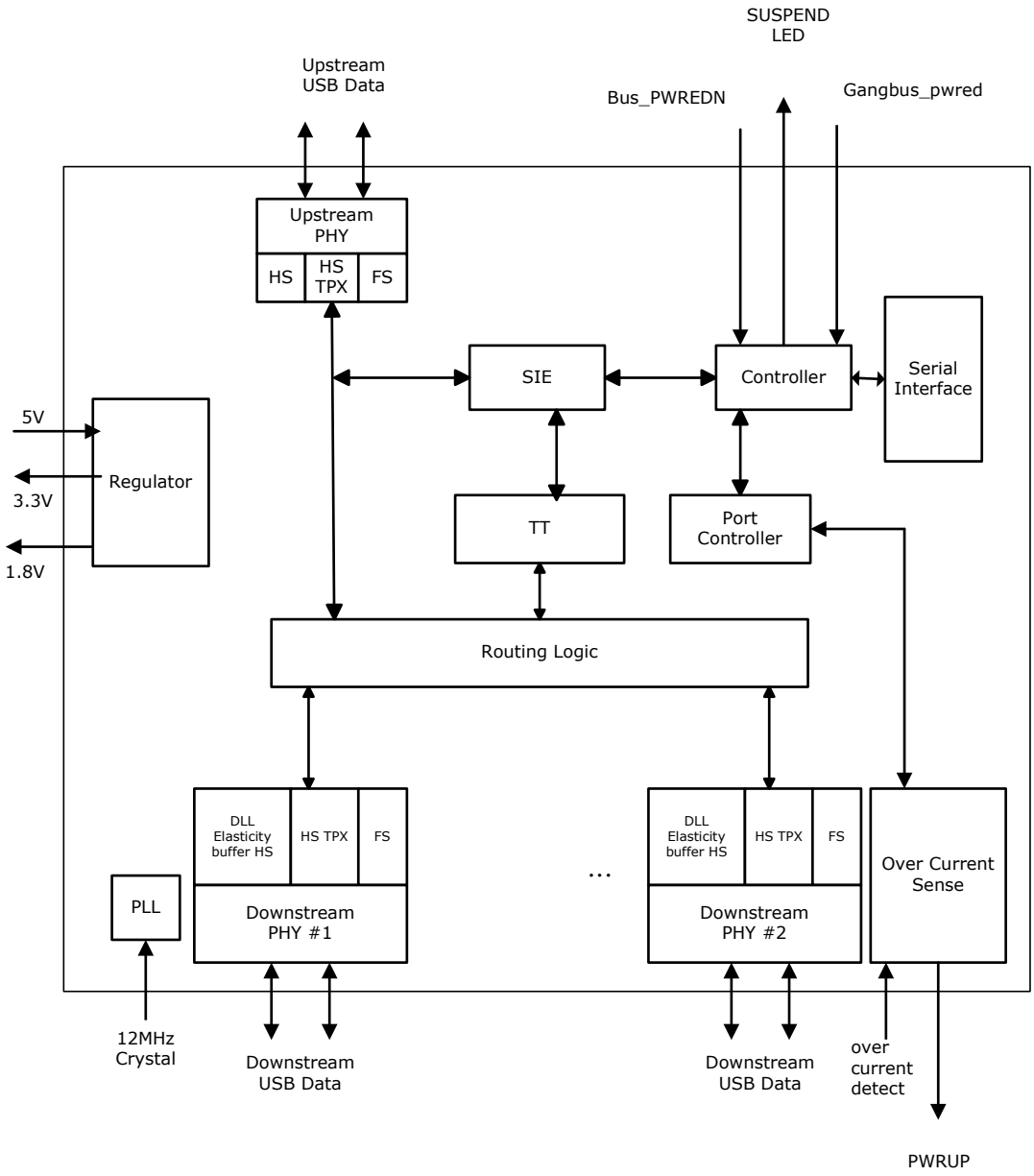
Pin #	Pin Name	I/O	Description
1	VSSH	Power	IO GND
2	UP_DM	I/O	Upstream Port USB data bus
3	UP_DP	I/O	Upstream Port USB data bus
4	AVDD	Power	UTMI Power input 3.3V
5	DP1_DM	I/O	Port1 USB bus
6	DP1_DP	I/O	Port1 USB bus
7	AVDD	Power	UTMI Power input 3.3V
8	UP_RREF	I	680Ω 1% current reference resistor
9	PVDD	Power	PLL VDD input 3.3V
10	XSCO	O	12MHz Crystal oscillator output
11	XSCI	I	12MHz Crystal oscillator input
12	PVSS	Power	OSC GND
13	DP2_DM	I/O	Port2 USB bus
14	DP2_DP	I/O	Port2 USB bus
15	AVDD	Power	UTMI Power input 3.3V
16	V18	Power	Voltage regulator output 1.8V
17	AVDD5V	Power	Voltage regulator input 5V
18	V33	Power	Voltage regulator output 3.3V
19	BUS_PWREDN	I	'1' = Self Powered '0' = Bus Powered
20	VDD	Power	Core Power input 1.8V
21	DP1_PWRUP	O	Port1 Power Enable; open collector output (require external pull up resistor to properly control power switch) '0' = power on '1' = power off
22	DP1_OVRCUR	I	Port 1 Over current; with internal pull up resistor '0' = over current '1' = not over current
23	NC		NC
24	SUSPEND	O	0' = Not Suspended '1' = Suspended
25	VDD	Power	Core Power input 1.8V
26	VSS	Power	Core GND
27	ChipResetN	I	Reset input. Active low when chip is reset to initial state

Pin #	Pin Name	I/O	Description
28	VDDH	Power	IO power input 3.3V
Pad	GND	GND	Ground

4. System Architecture and Reference Design

4.1 AU6259 Block Diagram

Figure 4.1 AU6259 Block Diagram



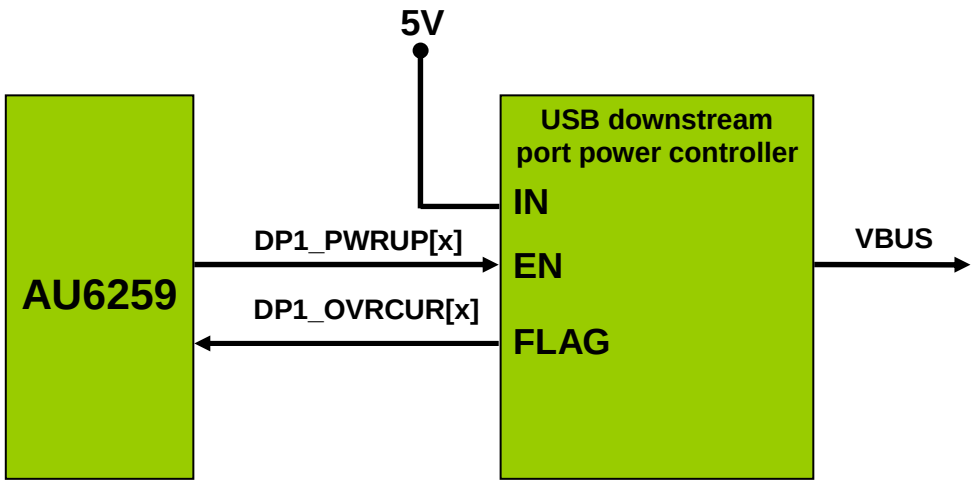
5. Battery Charging Support

5.1 General Description

All of downstream ports on AU6259 support Charging Host Port in compliance with the USB Battery Charging specification, version 1.2. AU6259 does not need enumerated for the port power to be enabled. Battery charging detection in S3, S4 and S5 system states is allowed as in the fully operational state.

A port that supports Charging Host Port must be able to supply 1.5 amps of current on VBUS. Therefore, the 5 volt power supply, port power control and over-current protection devices must be capable to handle the larger current demand compared to the Standard Host Port.

Figure 5.1 Battery Charging via external power supply



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{5IN}	Power Supply	-0.3 to 5.25	V
V_{DDH}	Power Supply	-0.3 to 3.6	V
V_{IN}	Input Signal Voltage	-0.3 to V_{DDH} +0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

6.2 Recommended Operating Conditions

Table 6.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{5IN}	Power Supply	4.75	5.0	5.25	V
V_{DDH}	Power Supply	3.0	3.3	3.6	V
V_{DD}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input Signal Voltage	-0.3		V_{DDH} +0.3	V
T_{OPR}	Operating Temperature	0		70	^{O}C

6.3 General DC Characteristics

Table 6.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	µA
I_{OZ}	Tri-state leakage current		-10	±1	10	µA
C_{IN}	Input capacitance	Pad Limit		2.8		pF
C_{OUT}	Output capacitance	Pad Limit		2.8		pF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		pF

6.4 DC Electrical Characteristics of 3.3V I/O Cells

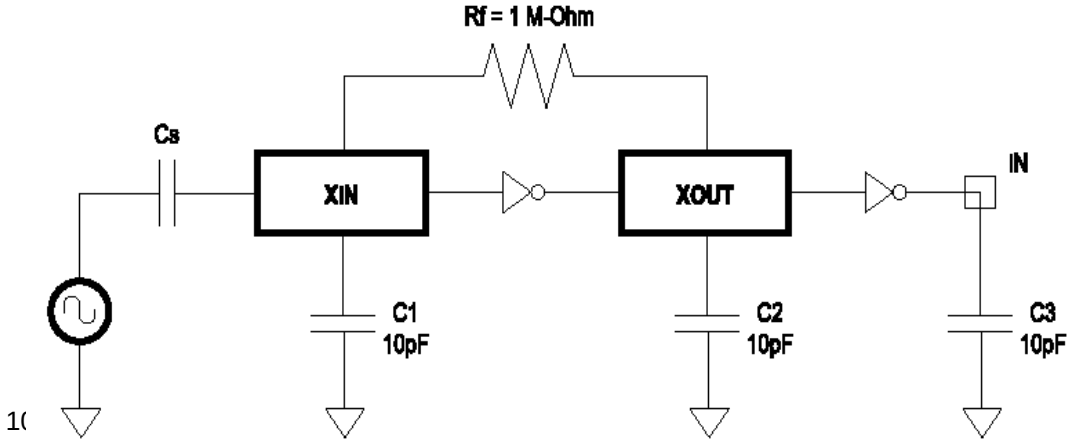
Table 6.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{DDH}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\lvert I_{ol} \rvert$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\lvert I_{oh} \rvert$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I_{in}	Input leakage current	V_{in}= V_{D33P} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

6.5 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2..

Figure 6.1 Crystal Oscillator Circuit Setup for Characterization



6.6 Bus Timing/Electrical Characteristics

Table 6.5 DC Electrical Characteristics

Input Levels for Low-/Full –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{IH}	High (Driven)	2.0		V
V_{IHZ}	High (floating)	2.7	3.6	V
V_{IL}	Low		0.8	V
V_{DI}	Differential Input Sensitivity	0.2		V
V_{CM}	Differential Common Mode Range	0.8	2.5	V

Input Levels for High –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HHSSQ}	High-speed squelch detection threshold (differential signal amplitude)	100	150	mV
V_{HSDSC}	High speed disconnect detection threshold (differential signal amplitude)	525	625	mV

Output Levels for Low-/Full-speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{OL}	Low	0.0	0.3	V
V_{OH}	High (driven)	2.8	3.6	V
V_{OSE1}	SE1	0.8		V
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V

Output Levels for High –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HSOI}	High-speed idle level	-10	10	mV
V_{HSOH}	High-speed data signaling high	360	440	mV
V_{HSOL}	High-speed data signaling low	-10	10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	700	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	-900	-500	mV

Terminations:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
R_{PU}	Bus Pull-up Resistor on Upstream Facing Port	1.425	1.575	kΩ
R_{PD}	Bus Pull-down Resistor on Upstream Facing Port	14.25	15.75	kΩ
Z_{INP}	Input impedance exclusive of pull-up/pull-down (for low-/full-speed)	300		kΩ
V_{TERM}	Termination voltage for upstream facing port pull-up (R_{PU})	3.0	3.6	V

Terminations in High-speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HSTERM}	Termination voltage in high-speed	-10	10	mV

Table 6.6 High-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{SHR}	Rise Time (10%-90%)	500		ps
T_{HSF}	Fall Time (10%-90%)	500		ps
Z_{HSDRV}	Driver Output Resistance (which also serves as high-speed termination)	40.5	49.5	Ω

Clock Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{HSDRAT}	High-speed Data Rate	479.76	480.24	Mb/s
T_{HSFRAM}	Micorframe Interval	124.9375	125.0625	μs
T_{HSRFI}	Consecutive Microframe Interval Difference		4 high-speed bit times	

Table 6.7 Full-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{FR}	Rise Time	4	20	Ns
T_{FF}	Fall Time	4	20	Ns
T_{FRFM}	Differential Rise and Fall Time Matching	90	111.11	%
Z_{ZRV}	Driver Output Resistance for driver which is not high-speed capable	28	44	Ω

Clock Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$T_{FDRATHS}$	Full-speed Data Rate for hubs and devices which are high-speed capable	11.994	12.006	Mb/s
T_{FDRATE}	Full-speed Data Rate for devices which are not high-speed capable	11.970	12.030	Mb/s
T_{FRAME}	Frame interval	0.9995	1.0005	Ms
T_{FRI}	Consecutive Frame Interval Jitter		42	ns

Full-speed Data Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{DJ1} T_{DJ2}	Source Jitter Total(including frequency tolerance): To Next Transition For Paired Transitions	-3.5 -4	-3.5 -4	ns ns
T_{FDEOP}	Source Jitter for Differential Transition to SE0 Transition	-2	5	ns
T_{JR1} T_{JR2}	Receiver Jitter: To Next Transition For Paired Transitions	-18.5 -9	-18.5 -9	ns ns
T_{FEPPT}	Source SE0 interval of EOP	160	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP	82		ns
T_{FST}	Width of SE0 interval during differential transition		14	ns

Table 6.8 Low-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{LR}	Rise Time	75	300	ns
T_{LF}	Fall Time	75	300	ns
T_{LRFM}	Differential Rise and Fall Time Matching	80	125	%
C_{LINUA}	Upstream Facing Port (w/cable, low-speed only)	200	450	pF

Clock Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$T_{LDRATHS}$	Low-speed Data Rate for hubs and devices which are high-speed capable	1.49925	1.50075	Mb/s
T_{LDRATE}	Low-speed Data Rate for devices which are not high-speed capable	1.4775	1.5225	Mb/s

Low-speed Data Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{UDJ1} T_{UDJ2}	Upstream facing port source Jitter Total(including frequency tolerance): To Next Transition For Paired Transitions	-95 -150	95 150	ns ns
T_{LDEOP}	Upstream facing port source Jitter for Differential Transition to SE0 Transition	-40	100	ns
T_{DJR1} T_{DJR2}	Upstream facing port differential Receiver Jitter: To Next Transition For Paired Transitions	-75 -45	75 45	ns ns
T_{DDJ1} T_{DDJ2}	Upstream facing port differential Receiver Jitter: To Next Transition For Paired Transitions	-25 -14	25 14	ns ns
T_{UJR1} T_{UJR2}	Downstream facing port Differential Receiver Jitter: To Next Transition For Paired Transitions	-152 -200	152 200	ns ns
T_{LEOPT}	Source SE0 interval of EOP	1.25	1.50	μs
T_{LEOPR}	Receiver SE0 interval of EOP	670		ns
T_{LST}	Width of SE0 interval during differential transition		210	ns

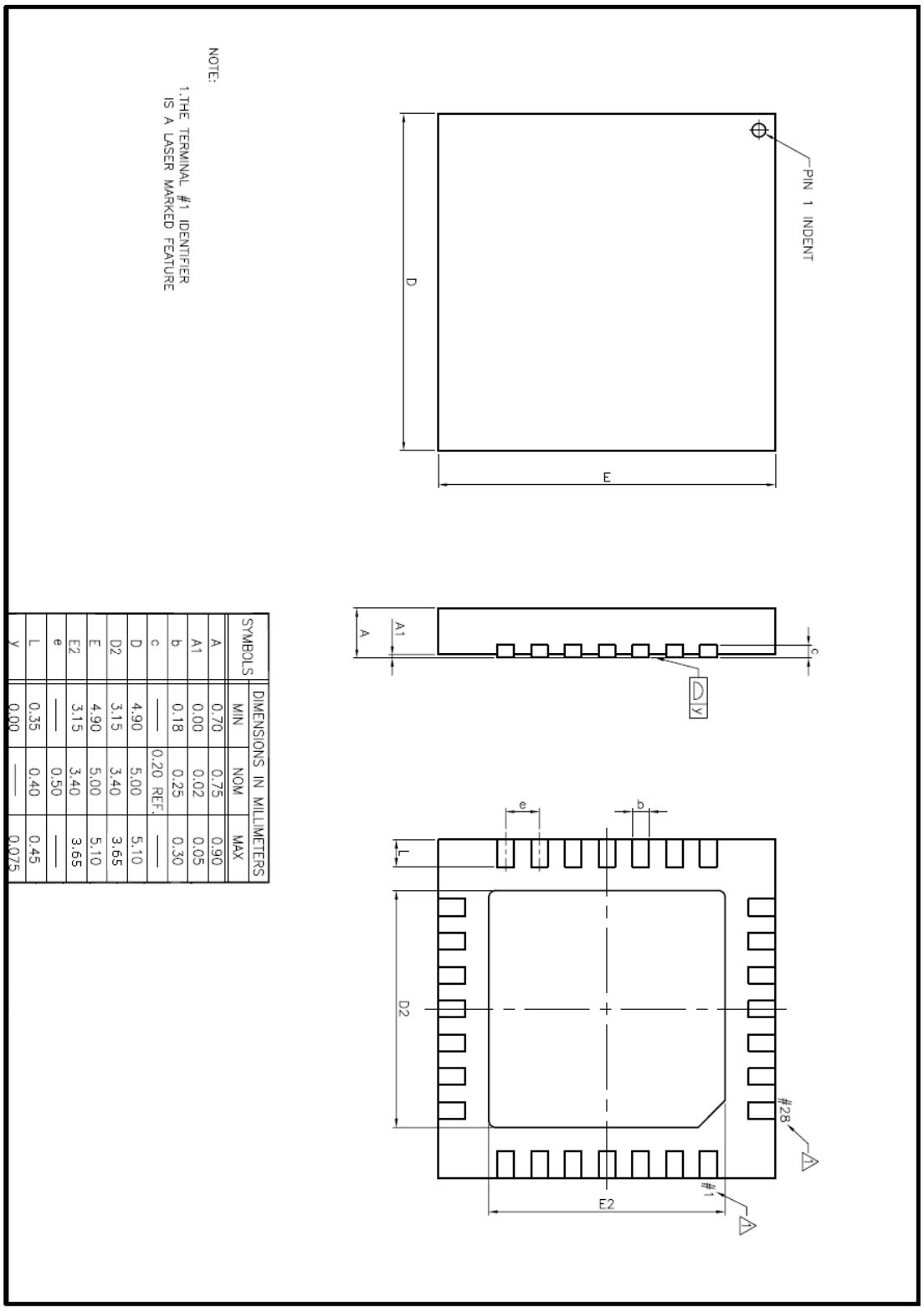
6.7 Power Consumption Note

Table 6.9 Power Consumption Note

Status	Condition			Idle	Operating (Reading/Writing)	Unit
	Active Ports	Host	Device			
Suspend				1.04	N/A	mA
Active	2	F	F	62	63	mA
		H	H	65	71	mA
		H	F	63	65	mA
	1	F	F	55	56	mA
		H	H	56	58	mA
		H	F	56	57	mA
	No Device	F	None	46	N/A	mA
		H	None	45	N/A	mA

7. Mechanical Information

Figure 7.1 28 QFN Mechanical Information Diagram



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	----	0.20 REF.	----
D	4.90	5.00	5.10
D2	3.15	3.40	3.65
E	4.90	5.00	5.10
E2	3.15	3.40	3.65
e	----	0.50	----
L	0.35	0.40	0.45
y	0.00	----	0.075

8. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

SIE	Serial Interface Engine
UTMI	USB Transceiver Macrocell Interface

About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.